

CMOS Duobinary Transceiver for Multigigabit Communications

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Abstract

This work presents a CMOS transceiver for amplitude duobinary modulation over an equalized 50-m step-index plastic optical fiber (SI-POF). Both duobinary precoder and decoder have been fabricated in 0.18- μm CMOS technology, enabling a bandlimited system of 700 MHz to operate at 3.125 Gbps with a consumption of 28.4 mW.

Introduction

Optical fibers have emerged as an interesting option instead of copper as transmission channel in short-range communications due to their excellent mechanical features. SI-POF is lightweight, compact, robust when bent and its large core makes it easy to handle and install. However, some kind of signal correction is necessary to compensate its narrow bandwidth-length product of 45 MHz x 100 m, in order to enable SI-POF for multigigabit applications.

An interesting possibility in this direction is the use of data formats different from traditional non-return-to-zero (NRZ) modulation. Multilevel modulation allows an increase of the data rate at the expense of design complexity of both emitter and receiver, as well as signal-to-noise ratio (SNR) degradation. In this way, the choice of duobinary modulation is a very good option. It is a modulation format that doubles the data rate with respect to NRZ by simple and low-power circuitry, without suffering as much SNR penalty as other amplitude modulation formats, like 4-PAM [1].

Duobinary Technique

Inter-symbol interference (ISI) is an overlapping in time between consecutive transmitted bits that happens when the spectral components of the transmitted signal are above the cut-off frequency of the channel. Duobinary modulation takes advantage of ISI, assuming that all the received symbols suffer from it.

Fig. 1 shows the block diagram of the amplitude duobinary transmission system. A precoder processes a bit sequence and the clock signal according to $\text{PRE}(t) = \text{PRE}(t-T_b) \oplus \text{IN}(t)$, where T_b is the bit period and \oplus denotes the logic XOR operation. The output of the precoder, PRE, is also NRZ modulated and it is sent through a bandlimited channel and a front-end. Due to ISI, the front-end output will be a distorted signal DUO, duobinary modulated, $\text{DUO}(t) = \frac{1}{2} [\text{PRE}(t) + \text{PRE}(t-T_b)]$. Finally, signal DUO, which is a 3-level signal, must be decoded in the receiver to recover the original bit sequence. Table I contains the truth table of this decoding process Ψ : $\text{DEC}(t) = \Psi [\text{DUO}(t)] = \text{IN}(t)$.

An important feature of the proposed duobinary sequence is that it is correlated and hence not all transitions can occur. The result is that a duobinary signal has a power spectral density (PSD) equal than that of an NRZ signal with half the data rate [2].

Circuit description

The precoder box in Fig. 1 shows the block diagram of the implemented precoder. The data signal and the clock signal enter a two-input AND logic gate, whose output goes to a Flip Flop (FF) working as a frequency divider. The FF is formed by two D-latches in master-slave configuration with negative feedback. All the cells in this work have been implemented using SCL cells, achieving 30% higher data rate in comparison to CMOS static logic.

Table 1. Duobinary Truth Table.

IN(t)	PRE(t-T _b)	PRE(t)	DUO(t)	DEC(t)
0	0	0	0	0
	1	1	1	
1	0	1	½	1
	1	0		

The channel is a 50-m Mitsubishi GH SI-POF, whereas the front-end is the combination of a large area Si PIN photodetector, a transimpedance amplifier and a continuous-time equalizer [3]. It all results in a system with 700 MHz bandwidth and 100 dB/decade roll-off. The effect of the SI-POF channel properly equalized has been simulated by means of a 5th order low-pass Bessel filter with 700 MHz bandwidth.

The duobinary decoder has been implemented with two voltage comparators and an XOR gate. The block diagram is shown in the decoder box of Fig. 1. The two voltage comparators have the same structure and they have been implemented with three differential amplifiers connected in cascade. The voltage ref_L in the first comparator must be adjusted to be between the logic levels 0 and $\frac{1}{2}$ of the DUO signal, whereas ref_H in the second one must be adjusted between the corresponding $\frac{1}{2}$ and 1 levels.

Results

The proposed duobinary precoder and decoder have been designed in a standard 0.18- μm CMOS technology fed with 1.8 V single supply. The precoder consumes 10.3 mW and the decoder 18.1 mW. The designs are tested for 3.125 Gbps with a pseudo-random bit sequence (PRBS) of $2^{31}-1$ bits. Fig. 2 shows the active zone of the dies. Fig. 3 shows the eye diagrams of the main parts of the transceiver: The precoder output, signal PRE; the TIA output (before equalization); the equalizer output, signal DUO; and finally, the decoder output, signal DEC. This output eye diagram presents an rms jitter of 3.6 ps and an aperture of 185 mV.

As it can be seen, a data rate of 3.125 Gbps can be achieved with a bandwidth of only 700 MHz. So, the equalization requirements of duobinary are relaxed in comparison with NRZ, which also alleviates power consumption of the equalizer and reduces the pernicious high-frequency noise.

Conclusion

This paper presents a novel CMOS transceiver that enables an equalized 50-m SI-POF channel to target 3.125 Gbps in a system limited in bandwidth at 700 MHz by means of amplitude duobinary modulation. It is designed with high-frequency cells implemented in 0.18- μm CMOS technology fed with 1.8 V, presenting a total consumption of only 28.4 mW.

REFERENCES

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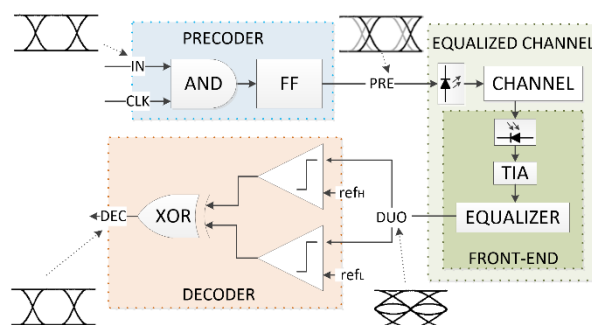


Fig. 1. Block diagram of the proposed duobinary system.

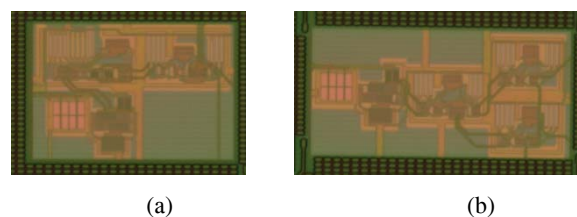


Fig. 2. Active zone of the fabricated ICs. (a) Duobinary precoder (140 μm x 95 μm) and (b) duobinary decoder (187 μm x 89 μm).

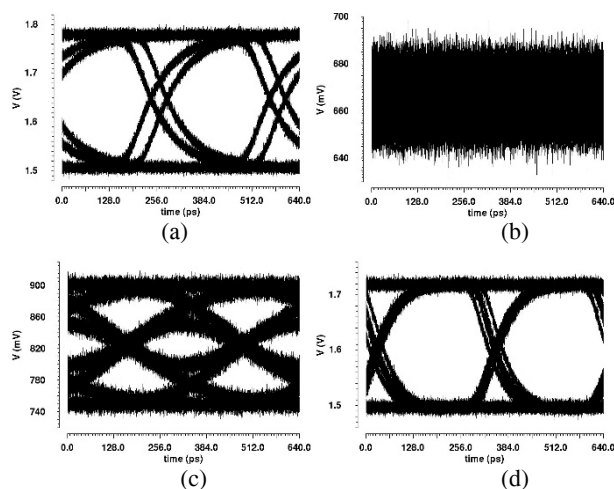


Fig. 3. Eye diagrams for 3.125 Gbps at (a) precoder output, signal PRE, (b) equalizer input, (c) equalizer output, signal DUO, (d) decoder output, signal DEC.