CMOS Receiver Front-End Architecture for High-Speed SI-POF Links

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Abstract

This works presents a new CMOS analog front-end for short-reach high-speed optical communications which compensates the limited bandwidth of POF channels and is suitable for the required large area photodetectorf The proposed pseudo-differential architecture, formed by a preamplifier and an equalizer, has been designed in a standard 0.18-μm CMOS process with a 1-V supply voltage targeting gigabit transmission for NRZ modulation. The preamplifier is based on the flipped voltage follower stage to attain a very low input resistance in order to handle the large phodiode capacitance (3 pF). The equalizer can adjust the high-frequency boosting and the gain, to compensate for the variation of the characteristics of the channel due to length of the fiber, connections, etc. causing subtantial changes of the fiber bandwidth. Reliable electrical models are employed for a Mitsubishi GH SI-POF with 10-m to 50-m length and for a S5972 silicon photodiode from Hamamatsu suitable for such a fiber due to its large diameter (0.8 mm) and responsivity at 650 nm (0.44A/W). The bandwidth of the received signal can be enhanced from 100 MHz to 1.4 GHz and from 300 MHz to 1.4 GHz for a 50-m and 10-m POF respectively. The proposed circuit shows a transimpedance of 41.5 dBΩ while the theoretical sensitivity from noise performance is below -7.5 dBm with a BER = 10^{-12}. The power consumption is below 16 mW from 1-V supply voltage. In conclusion it targets 1.25 Gbps through a 1-mm SI-POF up to 50-m length with a commercial Si PIN photodiode.

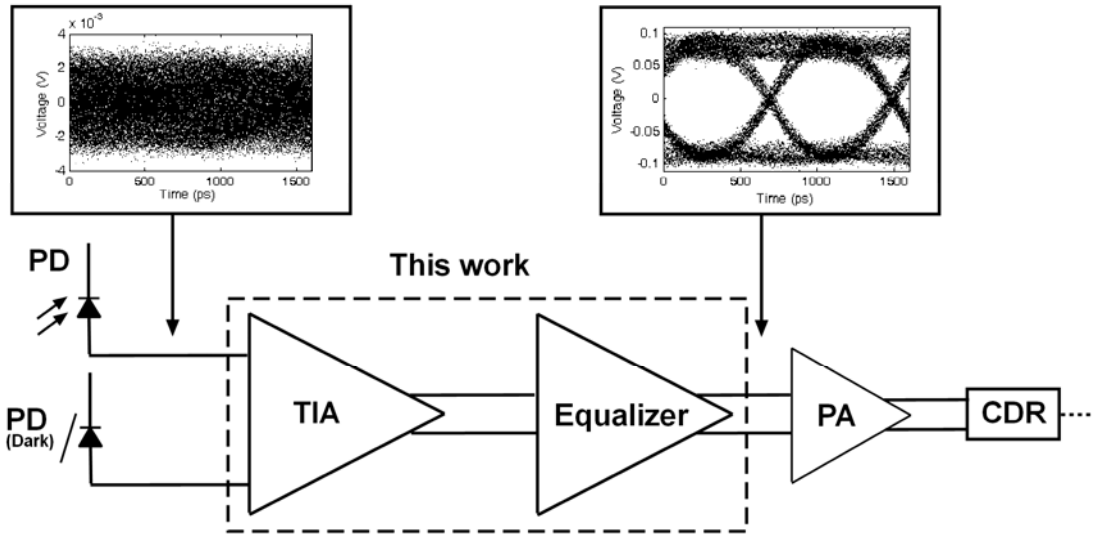

Fig. 1. Block diagram of the front-end for SI-POF links.