A Clock and Data Recovery Circuit for Optical Communications in 0.18 μm CMOS

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Abstract

The amount of data transmitted over the global communications networks has experienced a dramatic increase over the last years, mainly driven by the exponential growth of the Internet. For this reason, increasingly faster and more reliable circuits are needed to allow a correct performance at speeds in the range of the Gbps. The superior power characteristics and overall performance make optical fiber the preferred choice to implement the channel in communications links, giving rise to the concept of optical communications. Due to their bandwidth limitations, in a typical optical communcations link data cannot be transmitted with a timing reference; the clock signal that allows its correct interpretation has to be extracted at the receiver in a block called clock and data recovery circuit (CDR). Typically, a CDR circuit is a closed-loop system that generates an oscillating signal capable of tracking the phase of the incoming data stream; as well, it uses the generated clock signal to regenerate the data stream, minimising the effects of non-idealities during transmission. This paper presents the design of a CDR circuit intended to meet the 10GBase-LX4 Ethernet specifications for continuous operation at 3.125 GHz, designed in a standard 0.18 μm CMOS technology provided by UMC. A detailed description of the full CDR circuit and the different blocks taking part in it will be provided, emphasising the requirements that each of them must satisfy. Finally, the correct performance of the proposed CDR circuit will be analysed by means of an extensive set of post-layout simulations.

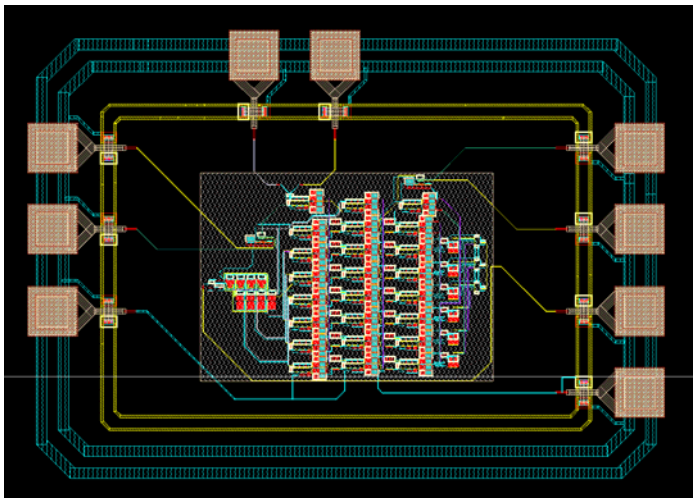

Fig. 1. Layout of the CDR circuit