

A 4- μ W 0.8-V Rail-to-Rail Input/Output CMOS Fully Differential OpAmp

M.R. Valero, S. Celma, N. Medrano

Grupo de Diseño Electrónico (GDE)
Instituto de Investigación en Ingeniería de Aragón (I3A)
Universidad de Zaragoza, ES-50009, Zaragoza, Spain.
e-mail: {mrvalero, scelma, nmedrano}@unizar.es

Abstract

This paper presents an ultra low power rail-to-rail input/output operational amplifier (OpAmp) designed in a low cost 0.18 μ m CMOS technology. In this OpAmp, rail-to-rail input operation is enabled by using complementary input pairs with gm control. To maximize the output swing a rail-to-rail output stage is employed. For low-voltage low-power operation, the operating transistors in the input and output stage are biased in the sub-threshold region. The simulated DC open loop gain is 51 dB, and the slew-rate is 0.04 V/ μ s with a 10 pF capacitive load connected to each of the amplifier outputs. For the same load, the simulated unity gain frequency is 131 kHz with a 64° phase margin. A common-mode feed-forward circuit (CMFF) increases CMRR, reducing drastically the variations in the output common mode voltage and keeping the DC gain almost constant. In fact, their relative error remains below 1.2 % for a (-20°C, +120°C) temperature span. In addition, the proposed OpAmp is very simple and consumes only 4 μ W at 0.8 V supply.

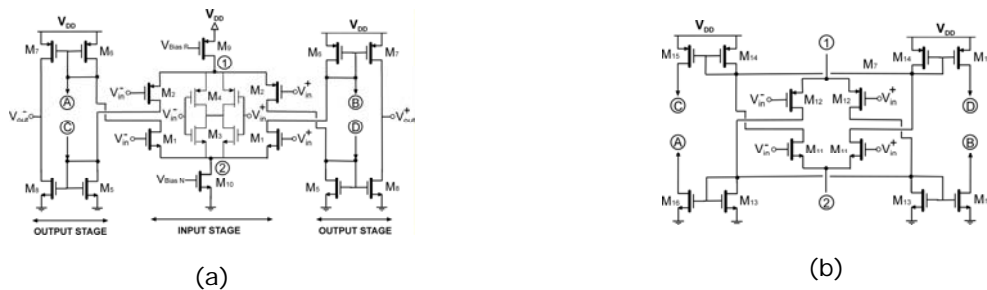


Figure 1. (a) Core of the proposed Operational Amplifier and (b) CMFF circuit.

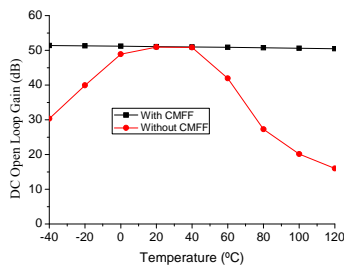


Figure 2. DC Open Loop Gain vs. temperature (with and without CMFF)

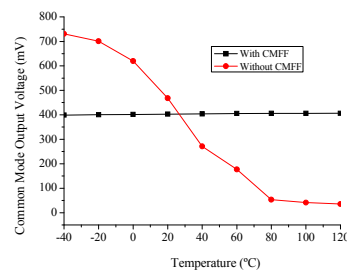


Figure 3. Common mode output voltage vs. temperature (with and without CMFF)