Design of a Digitally Programmable Phase Shifter for Active Antenna Arrays

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Abstract

This paper presents the design of a new phase shifter using CMOS technology of 65 nm, for its use in arrays of antennas opperating at the millimeter band (24 GHz). It is an active phase shifter digitally programmable using a 4-bit word.

Introduction

Antenna arrays are key elements in the new generation of wireless communication systems (5G) as well as in satellite communications (SATCOM), since they allow the radiation pattern to be ellectronically directed (beamforming) and to work with multiple beams simultaneously (Figure 1). Beamforming requires adjusting the phase of each of the radiant elements. So, phase shifters become essential components in an active antenna [1].

On the other hand, the millimetric band spectrum is still not saturated and there is more bandwidth available. In this band the signal is highly attenuated, reducing interferences and increasing the security at the same time. In adition, as the wavelength is small it is possible to diminish drastically the size of the elemental antennas, making more practical to build antenna arrays, without moving parts, which even allows their implementation on a PCB or its integration on a chip.

Proposed Topology

The topology proposed in this work for the phase shifter consists of two basic blocks: a quadrature signal generator and a variable gain amplifier (VGA) (Figure 2). To generate the cuadrature signal, a new quadrature all-pass differential filter (QAF), is proposed. Its performance is based on the orthogonal phase shift created in RLC resonators [2].

Then, using two 4-bit digitally progammable VGAs, each component of the I/Q signal is weighted independently [3]. Each VGA is made up of six blocks of three NMOS transistors, which allow the desired portion of the current to be diverted to the output. The remaining part will be driven to the supply by dummy transistors. The use of dummy transistors allows to keep constant the total number of transistors swiched on. In this way, the variations of the input impedance between different configurations are minimized and, consequently, the phase and gain errors will decrease.

Results

After adjusting the values of the different design variables by means of an iterative procedure, the values chosen for the final design are: $R = 95\ \Omega$, $L = 235$ pH, $C = 135$ fF, $L_0 = 219.5$ pH and $C_L = 151$ fF. For the transistors the choosen dimensioning has been $W/L = 1.1\ \mu m/120$ nm. Figure 3 shows the phase shifts obtained for a frequency of 24 GHz. It can be seen how for a weighted combination of the in-phase signal and the quadrature signal, the desired phase states are obtained with a practically constant gain in all of them. RMS errors at this frequency are 3.55º in phase and 0.78 dB in gain.

It has also been verified that the results obtained are maintained in a wide frequency range around the working frequency, from 14 GHz to 36 GHz. In this range, RMS errors are in between 3.45º and 8.81º for the phase, and 1.12 dB and 0.72 dB for the gain. The power consuption at 24 GHz is 5.2 mW. These resuls are of the order of those obtained in [2] and [4].

Conclusions

This work has addressed the initial stages of the design of a phase shifter, using a QAF to generate the in-phase and cuadrature signals, and two VGAs to weigh them. Its important to stand out the role of the dummy transistors, keeping the input and output impedances invariant between different configurations.

The desired results have been obtained with an RMS error of 3.55º in phase and 0.78 dB in gain at the work

frequency. It has also been verified that the different phase states are mantained in a wide frequency range.

Acknowledgments

This work is part of a project supported by the Ministry of Economy and Competitiveness (RTC2019-007039-7).

REFERENCES

[1]. BENSON, K. Phased Array Beamforming ICs Simplify Antenna Design. *Analog Dialogue*, 2019, vol. 53, no 1, p 10-13.

[2]. KOH, K., REBEIZ, G. M. 0.13-µm CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays. *IEEE Journal of Solid-State Circuits*, November, 2007, vol. 42, no. 11. pp. 2535-2546.

[3]. TSAI, J. H., LIN, C. L. A 40-GHz 4-Bit Digitally Controlled VGA with Low Phase Variation using 65-nm CMOS Process. *IEEE Microwave and Wireless Components Letters*, 2019, vol. 29, no. 11. pp. 729-732.

[4]. YU, Y., BALTUS, P. G. M., VAN ROERMUND, A. H. M. Integrated 60 GHz RF Beamforming in CMOS Springer. *A 60 GHz Active Phase Shifter Integrated with LNA*, 2011, pp. 59-80.

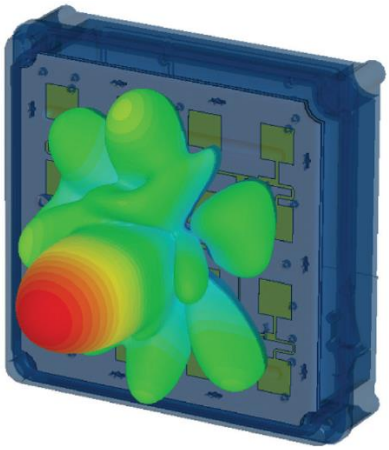

Figure 1. Phased array beamforming diagram. [1]

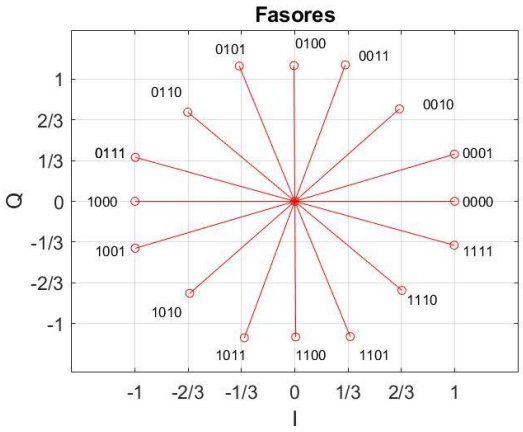

Figure 3. Phase shifts obtained at 24 GHz.

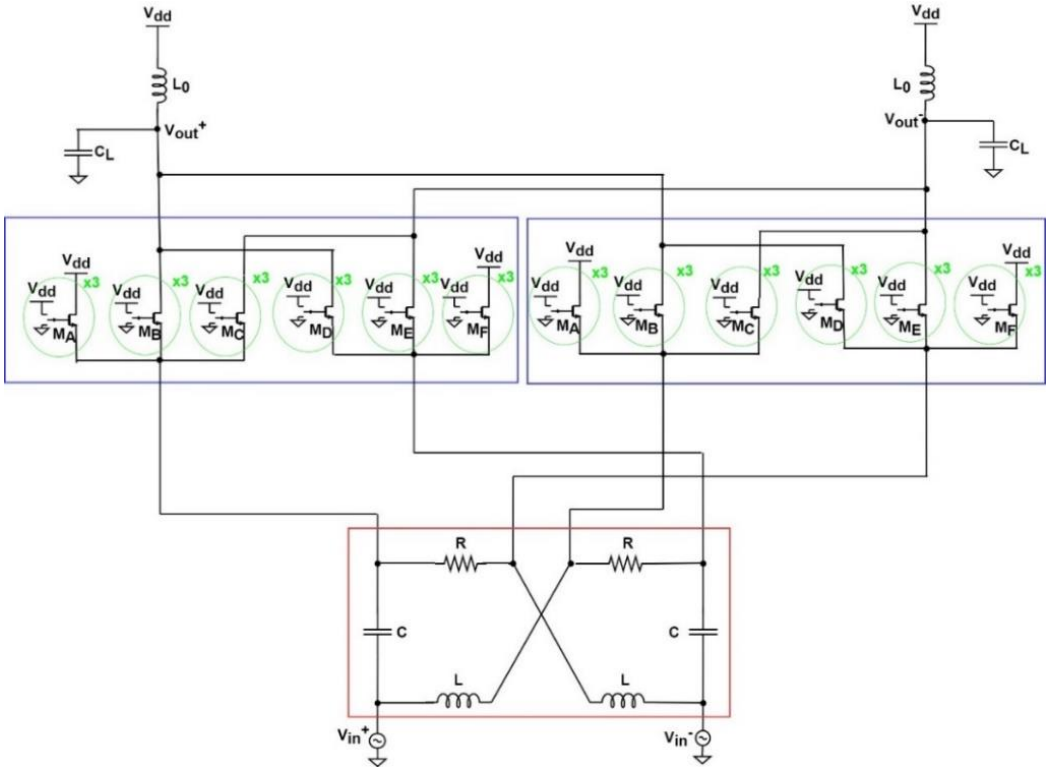

Figure 2. Phase shifter topology. The QAF is indicated by the red square and the VGAs by the blue ones.