A Digitally Programmable Analog Quadrature Sine Oscillator for on-chip Lock-In Measurement Systems

Alejandro Márquez, Nicolás Medrano, Belén Calvo, Pedro A. Martínez

Grupo de Diseño Electrónico (GDE) Instituto de Investigación en Ingeniería de Aragón (I3A) Universidad de Zaragoza, Mariano Esquillor s/n, 50018, Zaragoza, Spain. Tel. +34-976762707, e-mail: 612620@unizar.es

Abstract

This paper presents a CMOS 1.8V-180nm analog quadrature sine oscillator. Thanks to a custom 12-bit bidirectional DAC-based architecture, the frequency can be digitally programmed over two decades with high accuracy, making it suitable as the actuation system in low-cost high-performance embedded lock-in measurement systems.

Introduction

Lock-in amplifiers (LIA) are a powerful technique to recover information from sensors with small amplitudes or even showing a response buried in larger noise signals. Current commercial LIAs are heavy and power-hungry. Recently, low-voltage implementations have been proven feasible, but still are not marketed in an integrated manner and, in fact, only a few integrated versions have been reported to date. Previous work from authors proved the implementation of a 1.8V 0.18um CMOS dual phase read-out LIA channel [1].

For the actuation system a quadrature sinusoidal analog oscillator with a new high-resolution digitally tunable frequency system was specifically developed using COTS, since existing designs were not a feasible solution for low-powered systems either due to the high consumption and/or limited tunability [2]. Thus, to attain a complete on-chip LIA instrument, its 1.8V 0.18um CMOS design, complying with key performances including low power and reduced size while preserving a high resolution digitally programmable frequency is due.

Proposed System Performance

The proposed actuation system is shown in Figure 1. Following the strategy in [2], to attain a low-voltage low-power structure, it is an analog oscillator scheme using operational amplifiers as active cells, but using 12-bit digital-to-analog converters (DACs) to achieve precise resistance modifications. The DAC block diagram and detailed implementation at transistor level are shown in Figures 2 and 3

respectively. To attain a compact but accurate structure, the proposed DAC is divided into two segments: the 4 Most Significant Bits (MSB) are decoded to a thermometer code driving 16 unitary Z outputs in a second generation current conveyor (CCII) acting as a bidirectional current-steering architecture. The Least Significant Bit (LSB) segment is an 8-bit CMOS R/2-R ladder.

Figure 4 shows the output frequency programmability: frequency can be varied in two orders of magnitude, achieving high frequency accuracy. Figure 5 shows the quadrature sine wave outputs $V_{\rm O}$, $V_{\rm O1}$ at 10.88 kHz. These signals present identical amplitude value, with less than 0.3° phase error and the difference between the first and second harmonic is larger than 40 dB.

Conclusions

The use of a custom 12-bit bidirectional DAC-based architecture allows selecting the operating frequency in two decades with high accuracy, overcoming the intrinsic limitations from classical low-power analog oscillators in terms of frequency span and resolution. Additionally, the system can be straightforwardly controlled by low-cost low-power embedded microcontrollers. These features pave the way towards the accomplishment of general purpose fully integrated dual lock-in amplifiers, allowing to exploit their signal recovery features in those environments where expensive, mains powered bulky commercial LIAs become unsuitable.

REFERENCES

- [1]. GARCÍA-ROMEO, D., VALERO, M. R., MEDRANO, N., CALVO, B., and CELMA, S. A High Performance LIA-Based Interface for Battery Powered Sensing Devices. Sensors-Basel. 2015, 10, 25260-25275.
- [2]. GARCÍA-ROMEO, D., MARTÍNEZ, P.A., CALVO, B., and MEDRANO, N. High Resolution Analog Quadrature Sine Oscillator for Lock-In Amplifiers Applications. *Proceedings of the IEEE Sensors Conference*. Valencia, Spain, 2014.

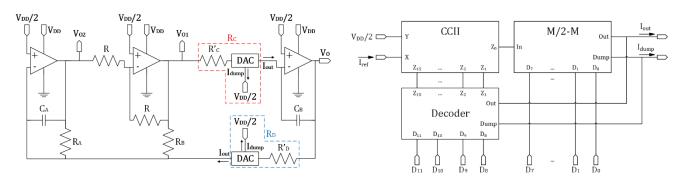


Figure 1. Proposed analog frequency programmable quadrature sine oscillator

Figure 2. DAC block diagram

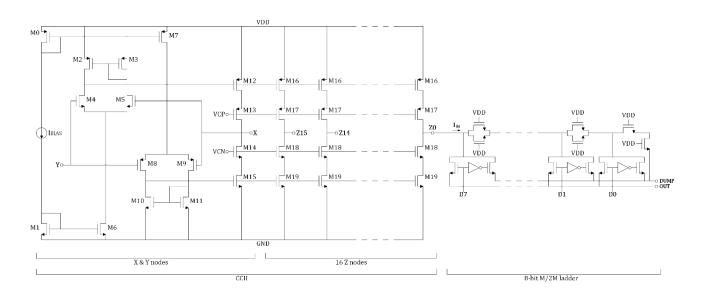


Figure 3. DAC detailed implementation at transistor level

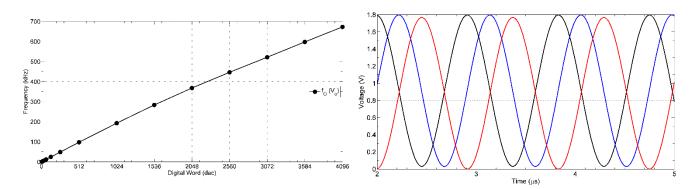


Figure 4. Output frequency programmability

Figure 5. Quadrature sine wave outputs V_0 (blue) and V_{01} (black) at 10.88 kHz