A 180nm CMOS Capacitorless Low Drop-Out Regulator for Battery-operated Systems

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Abstract

This paper presents a fully-integrated 180nm CMOS low drop-out regulator based on a simple telescopic cascode-compensated amplifier driving a PMOS pass-device. It provides a high precision 1.8V output voltage for battery voltages from 3.6V to 1.93V up to a 50mA load current with only 22µA quiescent current.

Motivation

The portable sensor market is pushing towards complete system-on-chip (SoC) solutions. One essential subsystem is the power management unit, where low drop-out (LDO) regulators play a key role delivering, under variations of load current I_L and battery voltage V_{BAT}, a stable power supply V_{out}. The goal of this work is the design of a LDO regulator to power both the read out and actuation electronics of a battery-compatible front-end sensor interface based on integrated analog lock-in amplifiers [1], with the aim to attain a forthcoming SoC CMOS system. The LDO specifications are fixed to: design in a low cost 0.18µm CMOS process with an output voltage of 1.8V from a 3.6V battery-compatible input voltage, maximum load current of 50mA and maximum 50pF load capacitor. Besides, it must comply with the two critical requirements of portable systems, i.e. reduced area and quiescent current, while maintaining good regulating performance, stability and fast response times, a challenging task with an on-chip approach [2].

Proposed LDO

The proposed LDO is shown in Figure 1. The external V_{ref} is set to 1.2V, the size of the PMOS pass transistor M_{PASS} is (W/L)=(9.5mm/0.34µm), and the feedback resistances are R_{fb1}=60kΩ, R_{fb2}=120kΩ, realized using identical diode-connected PMOS to optimize area. To attain high precision regulation with minimum power consumption, a single stage telescopic cascode error amplifier biased at 10µA is used. Cascode compensation, using a single Cc capacitor is adopted, thus achieving higher speed and power supply rejection (PSR) compared to the commonly used Miller compensation. To enhance the transient behaviour, a very simple dynamically biased current sink path is added, which is only active when the load current varies from high to low, helping to discharge the path formed by (R_{fb1}+R_{fb2}) and C_L.

The LDO main performances are summarized on Table 1. It provides 1.8V output with 0.008% precision for input voltages V_{BAT}=1.93V-3.6V up to 50mA load current with a total quiescent current of 22µA. Line regulation is shown in Figure 2, for I_L=50mA (worst case); load regulation for V_{BAT}=2.1V (worst case) is shown in Figure 3. Figure 4 shows the open loop frequency performance with Cc=8.5pF to ensure PM>60º over all the operating conditions. Figure 5 shows the full load transient response, displaying the benefit of the current sink path.

Conclusions

A high-performance fully-integrated LDO has been designed in 180nm CMOS. Compared to previous implementations with similar specifications [2-3], it attains a good trade-off between regulation performance, power, size and time response.

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This work was supported in part by MINECO-FEDER (TEC2015-65750-R)

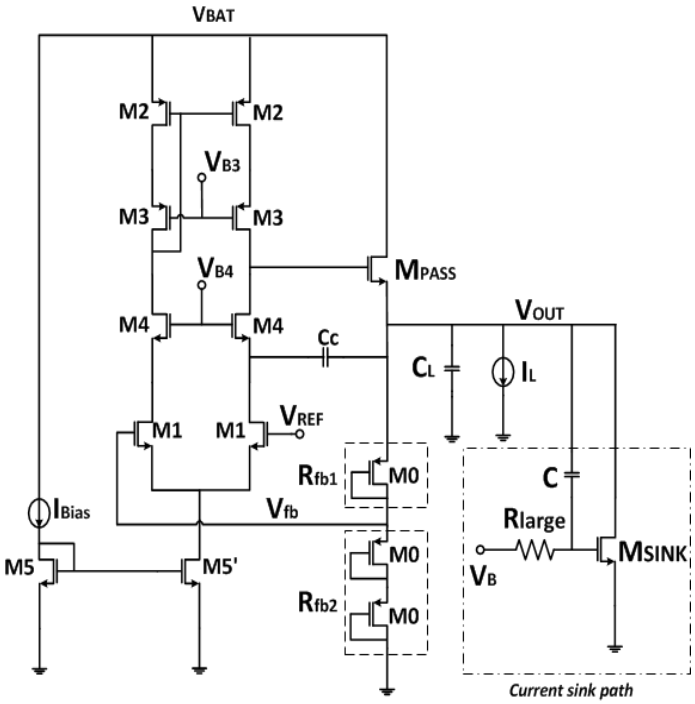

Figure 1: Schematic of the proposed CMOS LDO

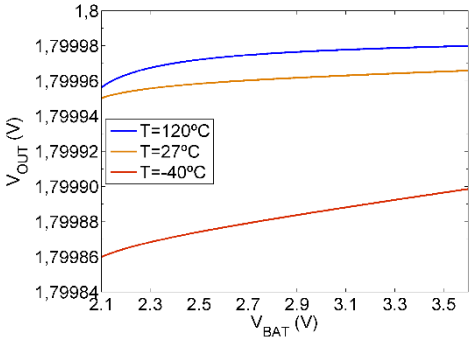

Figure 2: Static Line regulation, I_L=50mA

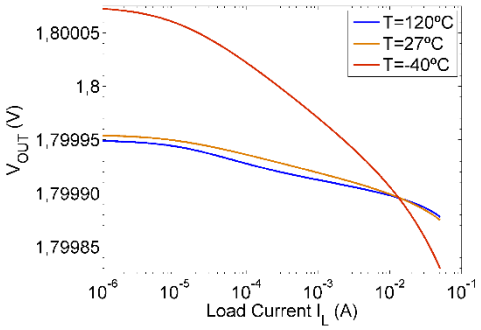

Figure 3: Static Load regulation, V_{BAT}=2.1V

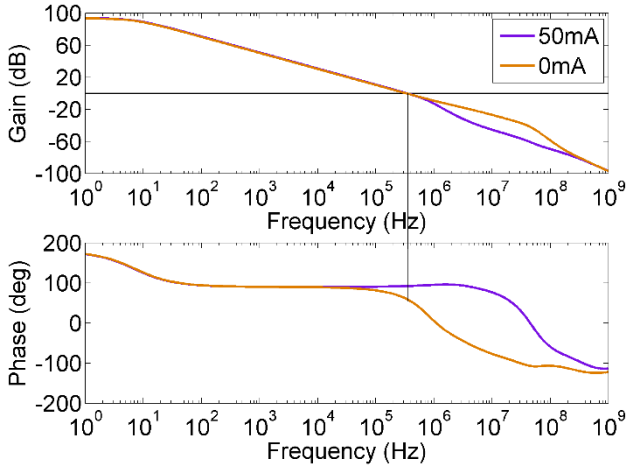

Figure 4: Open-loop frequency response, V_{BAT}=2.1V

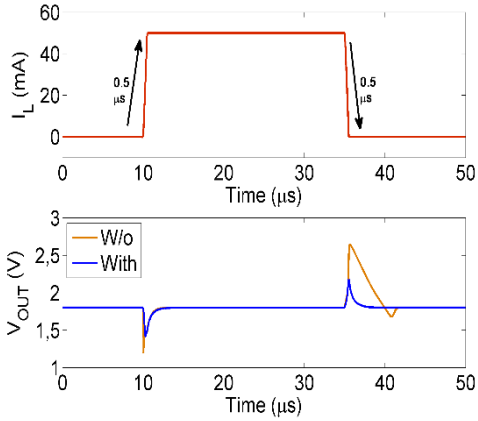

Figure 5: Full load transient w/o and with current sink path, V_{BAT}=3.6V

Table 1: Comparison of CMOS capacitor-less LDO performances

Parameter	*This work, sim*	*[2], 2007, exp*	*[3], 2011, exp*
Technology (µm)	0.18	0.35	0.35
V_{in} (V)	1.93 – 3.6	3	1.642 – 5
V_{out} (V)	1.8	2.8	1.5
V_{do} (mV)@$I_{L,max}$	130@50mA	200@50mA	142@100mA
I_q (µA)	22	65	27
C_L (pF)	50	100	100
Line Regulation (mV/V)	0.0087	~23	1.046
Load Regulation (mV/mA)	0.0036	~0.56	0.0752
Full load settling time (µs)	3	15	1 (I_L:0 to 100mA)
PSR (dB)	-62@1kHz	-57@1kHz	60.6@1kHz