Transimpedance Amplifier for Short-Reach SI-POF Links

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Abstract

This paper presents the design of a low-power low-voltage transimpedance amplifier for short reach applications through low-cost step index plastic optical fiber. The amplifier has been designed in a 180 nm CMOS technology and dissipates 6 mW from a supply voltage of only 1 V. The design achieves 1.25 Gb/s through 50 m POF and a sensitivity of -20 dBm considering a 10^{-12} BER.

Introduction

Transmitting data is essential in today's world. We are always connected and demanding a huge amount of information that grows every day. To carry all that information, the communication systems must be able to work at very high data rates. The main limitations are due to the channel, through which the information is transmitted, since the already installed copper-based channels cannot transmit data at several Gb/s [1].

Plastic optic fiber (POF) can provide a higher data rate than copper cables, it is also lighter, more flexible, and it is inmune to electromagnetic interferences, so it can be installed using the already existing electrical canalizations. Compared to glass optic fiber, its core is wider (1 mm compared to 10 - 100 μm), making POF more robust and easier to manipulate, which reduces the costs of installation and maintenance and makes POF an excellent candidate for short distance applications, such as home networks, or in the automotive industry.

On the contrary, POF suffers from high attenuation (0.2 dB/m at 650 nm) and a large area photodiode (PD) for high-efficiency light coupling is required, which will have an important parasitic capacitance. To overcome these limitations and increase the transmission length up to 50 m, highly sensitive optical receivers suitable for large area PDs have to be used [2].

In this paper we present the design of a transimpedance amplifier (TIA) that fulfills the needs for a data rate of 1.25 Gb/s and achieves a sensitivity of -20 dBm. It has been designed to be connected to an external silicon PD of 1-mm diameter with a responsivity of 0.44 A/W and a parasitic capacitance of 3 pF.

Circuit Design

Due to the high capacitance of the PD, the input impedance of the first stage of the optical receiver, the TIA, must be small. This reduces the topologies that can be used to: (i) an open loop topology with a common-gate stage (or variations of it, such as the regulated cascode); (ii) a shunt-feedback topology, which can be represented by an open loop voltage amplifier with a negative feedback network, as can be seen in Figure 1. The second one offers a higher transimpedance and the trade-offs between noise, bandwidth and transimpedance are not as tight as they are in open loop configurations. Because of that, it is the most popular TIA configuration in latest publications [3], [4], and it has been chosen for the design of the TIA presented in this work.

The transimpedance of the feedback TIA is

$$R_T(s) = -\frac{A}{A+1}\frac{R_F}{1+\frac{R_F C_{PD}}{A+1}s}$$

Where A is the module of the open loop gain of the amplifier, R_F the feedback resistor, and C_{PD} the parasitic capacitance of the photodiode.

The easiest way to implement the amplifier is a common-source (CS) stage. However, as the gain is too small, it is not possible to obtain the performance needed for POF applications, and more gain stages are needed. In this work, we propose three cascaded CS stages, which are suitable for low-voltage operation, using an NMOS (M_{iN}) as the amplifying element and a PMOS (M_{iP}) in the triode region in each stage (Figure 2).

Results

Simulations have been carried out using Spectre with a BSIM3v3.2 level 53 transistor model for a standard 180-nm CMOS technology. As the results depend on the PD, we have chosen a Hamamatsu silicon 5972 photodiode, which can be electrically modeled as a 3 pF capacitor. To optimize the input range we have set the output DC voltage at 750 mV, which is in the middle of the NMOS threshold voltage (500 mV) and the supply voltage (1 V).

The TIA presents a 1 GHz bandwidth and a transimpedance of 69 dBΩ, while the power consumption is of only 6 mW. With a noise simulation, the sensitivity can be calculated, obtaining a value of -20 dBm. An eye diagram with an input optical power of -20 dBm is shown in Figure 3. Furthermore, Montecarlo simulations have also been carried out for process variations and mismatch, in order to make further measurements of the behavior of the TIA. The results (Figure 4) show a standard deviation from the simulated results of approximately 15 %.

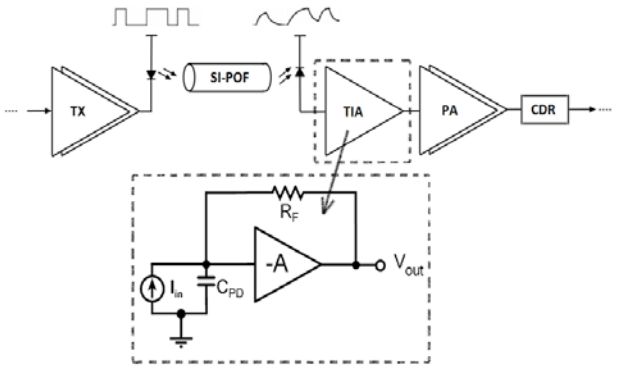

Figure 1. Block diagram of a SI-POF communication system and feedback TIA conceptual circuit.

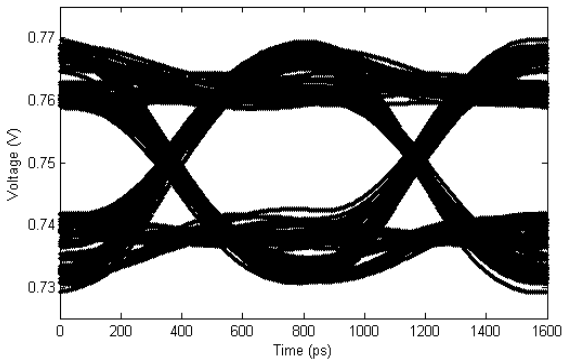

Figure 3. Eye diagram with an input optical power of -20 dBm and 1.25 Gb/s NRZ PRBS.

Conclusions

The proposed TIA overcomes both the high PD capacitance, achieving a 1 GHz bandwidth, and the high POF attenuation, presenting a transimpedance of 69 dBΩ and a sensitivity of -20 dBm. This performance should be enough for a data transmission through 50 m of POF. It is also suitable for low-power applications, since it consumes only 6 mW, and because of the supply voltage is of only 1 V, it is compatible with the most modern CMOS technologies.

References

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[3]. XUEBEI YANG, A. BABAKHANI. "A 2.5 Gb/s 0.38mm^2 optical receiver with integrated photodiodes in 0.18um CMOS SOI". In: *2014 IEEE MTT-S International Microwave Symposium (IMS).* Piscataway: IEEE, 2014, pp. 1-4.

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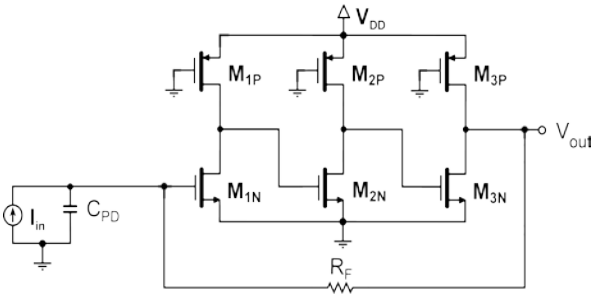

Figure 2. Topology of the proposed TIA.

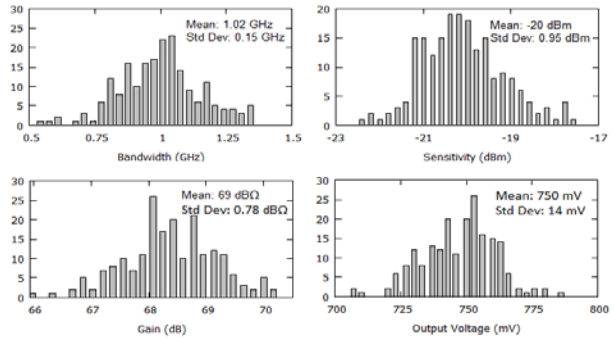

Figure 4. Montecarlo simulation results with UMC L180 MM/RF 1.8/3.3 V 1P6M technology.