A Double Loop Continuous-Time Adaptive Equalizer

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Abstract

This paper presents an adaptive equalizer for short-haul gigabit optical communications. It includes two adaptation loops to compensate the changes in level and spectrum of the input signal. It consumes 29.3 mW for a 1.25 Gb/s signal, transmitted through a 50-m length 1-mm core SI-POF.

Introduction

An obvious growing interest exists today in low-cost optical communication systems for consumer applications. Step-index plastic optical fibers (SI-POFs) are here preferred better than coaxial cable or glass optical fibers because they reduce the global cost and provide better immunity to noisy electromagnetic interference and better security [1]. Even though POF is already commercially used at speeds up to 100 Mb/s [2, 3], its main disadvantage is the low bandwidth-length product approximately 45 MHz x 100 m [4].

Continuous-time equalization has been proposed as a good trade-off for low-power high-speed low-cost applications. This equalizer must be able to adapt its response to changes in the fiber due to temperature, material properties, length, and other kinds of effects. The characteristics of the fiber can affect the BW of the signal but also to its amplitude (fiber losses are 0.14 dB/m at 650 nm).

In this work we propose a low-voltage, low-power, fully-balanced continuous-time equalizer which includes two completely independent adaptation loops: one for the gain, and another for the boosting of the equalizer. First we describe the main blocks that make it up as well as the most important performances and finally, conclusions are drawn.

Equalizer Architecture

Fig. 1 shows the architecture of the adaptive equalizer. In the first place a line equalizer is able to compensate the response of the POF. An enhanced gain control method is combined with a high-frequency boosting control loop to adjust the response of the equalizer to fiber changes.

The proposed line equalizer is a fully balanced split-path topology with a partial positive feedback loop to increase the ratio between differential and common-mode gain [5]. Contrary to the degenerated differential pair, it provides completely decoupled controls of the gain and the zero with an even higher common-mode regection ratio (CMRR).

Equalizer must automatically detect and compensate for the channel high frequency losses. A feedback loop [6] based on the spectrum balancing technique has been implemented, as shown in Fig. 1. It is formed by two low-pass filters and a power comparator. The power spectrum of the signal at the output of the equalizer is compared with the ideal one defined by a $sinc^2$ function for NRZ random sequence. The error signal, V_C, increases or decreases the boosting in the equalizer. A feedback topology, similar to that of the equalizer, is used to implement the first-order low-pass filters (LPFs) to achieve a high CMRR to perform the comparison of powers properly. The proposed power comparator [6] is based on the flipped-voltage follower differential pair. It avoids the use of high frequency rectifiers and precision error amplifiers, which are more difficult to design and power hungry; it also achieves a bigger input voltage swing than the standard power comparator based on the current-steering technique, overcoming the low-voltage limitation with lower power consumption.

As losses of the fiber can also affect the amplitude of the signal, it is necessary to include a gain adaptation loop. Two LPFs extract the low-frequency part of the slicer input and output signals. Then, a power comparator obtains the difference between the powers of the two quantities and generates a control signal to modify the gain of the line equalizer. The LPFs and the power comparator have been implemented using the same architectures as in the boosting adaptation loop. Also, the high CMRR of the LPFs ensure the same common-mode

for both comparator input signals, to properly perform the power comparison.

Preliminary Results

The proposed continuous-time adaptive equalizer has been designed in a standard 0.18-µm CMOS technology fed with only 1 V. The whole equalizer power consumption is approximately 29.3 mW, where 9.4 mW corresponds to the line equalizer, 4.9 mW to the boosting adaptation loop and 15 mW to the gain adaptation loop and the slicer.

The system can adjust its response to changes in the BW of the input signal from 100 MHz up to 400 MHz, (50-m down to 10-m POF). It can also adjust its response to changes in the level of the signal of up to 12 dB. These important results validate the effectiveness of the proposed architecture.

Fig. 2 compares how the output of the equalizer evolves when the amplitude of the input signal changes for our two adaptation loops equalizer and the same one but without gain adaptation loop. Fig. 3 shows the eye diagrams at the input and output of the circuit for two different channel lengths: 10 m and 50 m. We use a PRBS of 2^{31}-1 maximum length NRZ data stream at 1.25 Gb/s.

Conclusions

This paper presents a new low-voltage, high-frequency adaptive equalizer designed in a standard 0.18-µm CMOS technology. It compensates the low bandwidth of 1-mm SI-POF and adapts its boosting in answer to the variations of the characteristics of the fiber. It virtually compensates the PVT variations on the circuit due to the two independent adaptation loops included in the design: gain and boosting.

Moreover, the whole adaptive equalizer consumes less than 29.3 mW with a single supply voltage of only 1 V. These values are compatible with most modern low-cost standard digital nano-CMOS technologies, which impose 1-V operation in mixed analog-digital front-ends. The prototype achieves 1.25 Gb/s up to 50-m length of 1-mm SI-POF, making this approach attractive to implement gigabit transmission demanded by in-house networks.

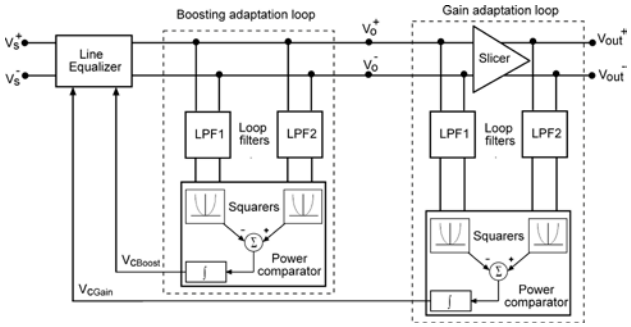
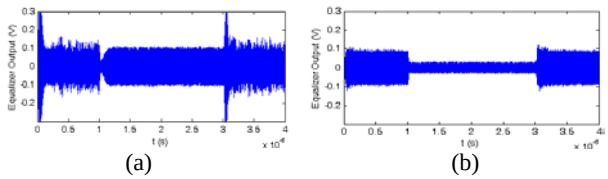


Fig. 1. Block diagram of the proposed adaptive equalizer.



(a) (b)

Fig. 2. Equalizer output signal when changes of 12 dB in the amplitude are produced (a) for the proposed equalizer, and (b) for an equalizer without gain loop.

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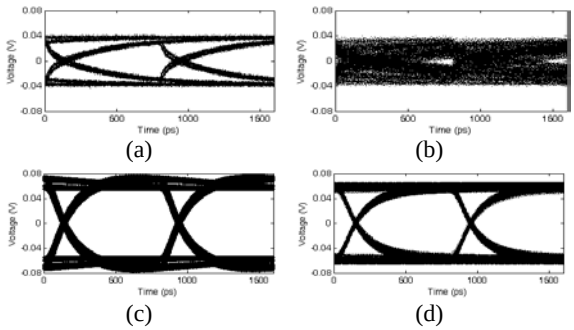

(a) (b) (c) (d)

Fig. 3. Eye diagrams at 1.25 Gb/s for (a) 10-m POF and (b) 50-m POF at the input of the circuit and for (c) 10-m POF and (d) 50-m POF at the output of the circuit.