A 1.25 Gb/s Fully Integrated Optical Receiver for SI-POF Applications

Cecilia Gimeno[1], Santiago Celma[1], Concepción Aldea[1], Ciaran Cahill[2]

[1] Afiliación: Group of Electronic Design
Instituto de Investigación en Ingeniería de Aragón (I3A).
Universidad de Zaragoza, Mariano Esquillor s/n, 50018, Zaragoza, Spain.
Tel. +34-976762707, Fax +34-976762043, e-mail: cegimeno@unizar.es
[2]Afiliación: Firecomms Ltd., Cork, Ireland

Abstract

This paper presents a 1.25 Gb/s fully integrated BiCMOS optical receiver for short reach applications through low-cost step index plastic optical fiber. The design achieves 1.25 Gb/s through 50 m POF with a power consumption of 148 mW and a sensitivity of -16.4 dBm for a BER of 10^{-12}.

Introduction

Optical communications has been widely used for high-speed digital data transmissions. Polymethyl-metacrilate ("plastic") step-index optical fibers (SI-POF) are preferred in this market since they are robust, light, reliable, easy to install and increasingly competitive in price.

Optical receivers with monolithically integrated photo detector have received a lot of research efforts recently [1-3] as they reduce the assembly costs, increase the reliability and eliminate the limitation imposed by packaging parasitics [3].

Unfortunately, the main disadvantage of SI-POF cable is its limited bandwidth-length product of approximately 45 MHz x 100 m. To obtain a simpler and cheaper communication system, NRZ modulation combined with equalization of the signal is proposed. Moreover, SI-POF links also suffer from high attenuation and losses. To increase the transmission length up to 50 m, highly sensitive optical receivers (-15 dBm for a transmitter power of 0 dBm) with large photodiodes have to be used.

For these reasons, we have designed a low noise, fully integrated analog front-end for short-reach high-speed optical communications that includes an equalizer to compensate the limited bandwidth of POF channels. The paper is laid out as follow. Section 2 describes the proposed fully integrated receiver. The most important simulated performances are summarized in Section 3. Finally, preliminary conclusions are drawn in Section 4.

Design

The architecture of the presented receiver can be seen in Figure 1. When light impinges on the integrated photodiode (PD), it is converted to a photocurrent. A dummy PD has been used to cancel the influence of the dark current and concomitant noise. The differential component of the photocurrent contains the wanted high-frequency data and needs to be amplified and converted to a voltage. This is accomplished in the transimpedance amplifier (TIA). In order not to amplify the offset voltage of the circuit, an offset compensation loop has been included. An automatic gain control loop adjusts the gain of the TIA. To extend the limited bandwidth of the POF an analog equalizer has been included in the receiver which boosts the high frequency component of the signal. The post amplifier amplifies the signal to obtain a signal with a swing of several 100 mV which is high enough for a clock-and data-recovery circuit to work with.

Results

The analog front-end has been designed in a 0.35 µm BiCMOS technology with a single supply voltage of 3.3 V. The front-end power consumption is 148 mW where 66.3 mW corresponds to the TIA, 42.6 mW to the line equalizer, and 39.2 mW to the postamplifier.

The BW of the received signal can be enhanced from less than 100 MHz (due to the limitations of the 50 m POF and the integrated PD) to 800 MHz. An error-free whole sensitivity of -16.4 dB is achieved. If the fiber length is 10 m, the sensitivity improves up to -21 dBm. These results validate the effectiveness of the proposed architecture. For 50 m SI-POF, Figure 2 (a) shows the simulated eye diagram at the input of the circuit and Figure 2 (b) shows the measured eye diagram at the output of the front-end for 1.25 Gb/s.

The main simulation results are summarized and compared with those of several previous results in Table 1. For this purpose a figure-of-merit (*FOM*) has been defined as follows

$$FOM = \log\left|\frac{Rate(Gbps)\cdot\log BER\cdot Sensitivity\ (dBm)\cdot PD\ Area\ (\mu m^2)}{Power(mW)}\right|$$

In this way, our proposed front-end provides a *FOM* of 5.42 which is better than the *FOM* obtained for the other receivers in Table 1, although [1], [2], and [3] do not need an equalizer to compensate the response of the POF because they use more expensive and therefore higher speed links. Moreover, in these circuits, the fiber-receiver coupling is worse due to the smaller photodiode diameter, demanding higher output laser power.

Conclusions

A fully integrated cost-effective optical receiver for low-cost short-range applications is presented. Preliminary simulation results show that the receiver achieves 1.25 Gb/s up to 50 m POF, making this approach attractive to implement gigabit transmission demanded by in-house networks.

References

[1] Chen, W.-Z., Huang, S.-H., Wu, G.-W., Liu, C.-C., Huang, Y.-T., Chin, C.-F., Cahng, W.-H., and Juang, Y.-Z. 2007. A 3.125 Gbps CMOS fully integrated optical receiver with adaptive analog equalizer. In *Proc. IEEE Asian Solid-State Circuits Conf.*,

[2] Hermans, C., Tavernier, F., and Steyaert, M. 2006. A gigabit optical receiver with monolithically integrated photodiode in 0.18 µm CMOS. In *Proc. ESSCIRC`06*.

[3] Dong, Y., and Martin, K. W. 2012. A high-speed fully-integrated POF receiver with large-area photo detectors in 65 nm CMOS. *IEEE Journal of Solid-State Circuits*. 47, 9 (Sep. 2012), 2080-2091.

[4] Atef, M., Swoboda, R., and Zimmermann, H. 2012. 1.25 Gbit/s over 50 m step-index plastic optical fiber using a fully integrated optical receiver with an integrated equalizer. *Journal of Lightwave Technology*. 30, 1, (Jan. 2012), 118-122.

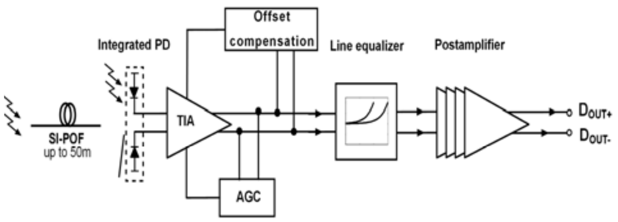
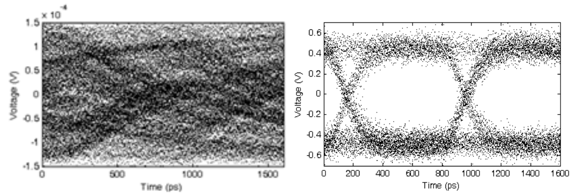


Figure 1. Topology of the presented optical receiver.



(a) (b)

Figure 2. Eye diagrams (a) at the input and (b) output of the front-end.

Table 1. Comparison with other works

	THIS WORK	[4], 2012	[3], 2012	[2], 2006	[1], 2007
Technology	0.35 µm BiCMOS	0.6 µm BiCMOS	0.065 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Rate	1.25 Gb/s	1 Gb/s	3.125 Gb/s	1.2 Gb/s	3.125 Gb/s
Fiber Length	(10-50 m)	50 m	30 m (GI)	-	-
PD diameter	0.4 mm	0.4 mm	0.25 mm	0.08 mm	0.065 mm
Power	148 mW	100 mW	50 mW	144 mW	175 mW
Voltage supply	3.3 V	3.3 V	1.2 V	1.2 V	3.3 V
Sensitivity	-16.41 dBm	-13.0 dBm	-3.8 dBm	-8 dBm	-4.2dBm (-7 dBm at 1.25 Gb/s)
BER	10^{-12}	10^{-9}	10^{-12}	10^{-12}	10^{-12}
FOM	5.42	5.27	5.25	3.7	3.58 (3.4)