Exploration of photonic networks on chip with the University of Ferrara

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Abstract

Modern chips include several processors that communicate through an interconnection network, which has a direct impact on system performance, power consumption and chip area. Recent research points out the great potential of optical networks to reduce on-chip communication latency and energy. We plan to explore this state-of-the-art field during an internship in the University of Ferrara.

Introduction

Computer capabilities grow with each new generation, but users keep on demanding higher speed and storage capacity, forcing manufacturers to constantly improve their designs. Nowadays, power is a rising concern that limits computer architecture development due to environmental concerns and the proliferation of battery-powered devices [4].

The current trend in system design relies on replication to achieve the required goals. One of the most common and efficient designs are Chip Multiprocessors (CMPs), which include in a single chip several processors that share the memory hierarchy through an interconnection network [1, 2, 3]. In this project, we are going to focus on this network on chip (NoC).

The importance of the interconnect is growing as the number of cores integrated in a chip increases. Communication between nodes can become a bottleneck and slow down performance improvement. The NoC also contributes with a substantial share to power consumption and chip area.

Traditionally, the NoC has been designed, implemented and evaluated assuming electronic routers and metal wires [5, 6, 7]. However, recent research on silicon nanophotonic technology demonstrates that all the elements needed to build an optical interconnection network can be integrated on a chip [8]. Optical NoCs is a fairly new field of research which has a lot of potential and many exciting ideas left to explore [9, 10, 11]. This work, developed in conjunction with the University of Ferrara, aims to deepen our understanding of photonic networks by studying their feasibility for future NoC architectures.

Details of the work to be performed

The collaboration will focus on the the system-level validation of an optical interconnect. We will determine if a fully optical interconnect is rewarding and evaluate utilization policies for hybrid electro-optical interconnects.

We will benchmark a hybrid electro-optical interconnection network and compare it to its fully electronic counterpart. There exist many comparison initiatives in the open literature, which always highlight the lower power dissipation of optical links [12, 13]. The main difference of this novel benchmarking initiative consists of a cross-layer analysis of the problem, ranging from technology, devices and circuitry (optical power loss modeling, placement and routing effects in the optical NoC, accurate RTL modelling of electro-optical interfaces, etc.) to a system-level perspective (definition and adaptation of the memory hierarchy, coherence policies, simulation of representative benchmarks, etc.)

The collaboration will range across these abstraction layers by exploiting the synergy of the involved partners, thus yielding a crossbenchmarking framework of uncommon accuracy. The University of

Ferrara (UNIFE) will cover the layers from technology to RTL, while the University of Zaragoza (UNIZAR) will cover the system-level design aspects.

In practice, two simulation frameworks will be used and their informative content will be made coherent with one another through an abstraction process that preserves accuracy. On one hand, a SystemC based simulation environment capable of capturing network interfacing effects will be developed and used by UNIFE. This framework will backannotate macromodels of physical information, such as insertion losses or delays. On the other hand, a system-level simulation framework will abstract the key RTL effects and enable to refer architectural features to their macroscopic performance implications. In the time frame of the collaboration, the two frameworks will be made aware of optical (and hybrid) interconnect technology, and coherent with one another. The expertise of UNIFE and UNIZAR in optical interconnection networks and memory hierarchy, respectively, guarantees that the collaboration will be extremely successful.

Conclusions

The specific goals we expect to achieve can be classified into two categories:

- From an architectural viewpoint, we will quantify the minimum distance beyond which an optical link becomes cost-effective over its electronic counterpart, quantify the buffering requirements at the network interfaces depending on network settings and assess how to implement flow control for an optical network.

- From a system-level viewpoint, we will customize the memory hierarchy for an optical interconnect, proposing utilization policies for hybrid interconnection networks and defining when to route a packet through a network vs. the other.

This collaboration project will ramp up our knowledge of optical NoCs and allow us to apply it to the interconnect-memory codesign. Furthermore, it will lay the foundations for a long-term collaboration between both research groups.

REFERENCES

[1] Wendel, D.F, et al. 2011. POWER7, a Highly Parallel, Scalable Multi-Core High End Server Processor. *IEEE Journal of Solid-State Circuits.*
[2] Howard J., et al. 2011. A 48-core ia-32 processor in 45 nm CMOS using on-die message-passing and DVFS for performance and power scaling. *IEEE Journal of Solid-State Circuits.*
[3] Nawathe U.G., et al. 2008. Implementation of an 8-core, 64-thread, power-efficient Sparc server on a chip. *IEEE Journal of Solid-State Circuits.*
[4] Chang L. el al. Strategies for Power-Efficient Computing Technologies. Proceedings of the IEEE, 2010.
[5] Dally W.J. and Towles B.. 2001. Route packets, not wires: on-chip interconnection networks. *Proc. 38Th Design Automation Conference.*
[6] Kumar R., et al. 2005. Interconnections in multi-core architectures: understanding mechanism, overheads, scaling. *Proc. 32Nd Annual International Symposium in Computer Architecture*.
[7] Ortín M., et al. 2013. Characterization and Cost-Efficient Selection of NoC Topologies for General Purpose CMPs. *7th International Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip*.
[8] Marris-Morini D. et al. 2011. HELIOS project: deliverable D010: state-of-the-art on Photonics on CMOS.
[9] Ramini L. and Bertozzi D. 2012. Power efficiency of wavelength-routed optical NoC topologies for global connectivity of 3D multi-core processors. In *Proceedings of the Fifth International Workshop on Network on Chip Architectures.*
[10] Ramini L., et al. 2012. Engineering a Bandwidth-Scalable Optical Layer for a 3D Multi-core Processor with Awareness of Layout Constraints. In *Proceedings of the Sixth International Symposium on Networks-on-Chip.*
[11] Parini A., et al. 2011. Abstract modelling of switching elements for optical networks-on-chip with technology platform awareness. In *Proceedings of the Fifth International Workshop on Interconnection Network Architecture: On-Chip, Multi-Chip.*
[12] Shacham A., et al. 2007. The case for low-power photonic networks on chip. In *Proceedings of the 44th annual Design Automation Conference*..
[13] Shacham A., et al. 2008. Photonic Networks-on-Chip for Future Generations of Chip Multiprocessors. *IEEE Transactions on Computers.*