Programmable all-optical logic gates based on semiconductor optical amplifiers

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Abstract

In this paper, we discuss the feasibility of optical programmable logic devices based on non-linear processing with semiconductor optical amplifiers. We carried out simulations of the architecture of an all-optical 4-bit Look-up Table, which is the basic logic element of larger-scale programmable devices, and experimental results from a proof-of-concept setup using commercially available devices. Experimental work with photonic integrated circuits to assess the feasibility of integration of such architectures is also presented.

Introduction

Network transparency has become a fundamental part of research in the field of optical communications over the last decade. While the speed of photonics continues increasing, electronics have reached a ceiling and struggle to keep up with modern networks routing demands. So far, this problem has been faced by parallelization of the processes; however, the higher rates of photonic devices would improve not only communications but other applications that require of high-speed data processing as well.

A number of elements, from basic logic gates to wavelength converters have been studied and demonstrated exploiting different optical nonlinear effects such as Four-Wave Mixing (FWM) [1], Cross Gain Modulation (XGM) [2, 3] and Cross Phase Modulation (XPM) [4]. These effects occur in several non-linear optical media, but are particularly efficient in Semiconductor Optical Amplifiers (SOA), limiting their potential for in-line amplification but also enabling their use for optical processing. Taking advantage of these effects several logic gates such as NOT, XOR [3], AND and NAND have been reported in literature, individually or in combination with others, in parallel or in cascade. However, most of the effort in this field has focused in performance and not in obtaining higher functionality. We believe this all-optical processing technology based on SOAs exhibits a great potential for future applications, and now that simple operations have been demonstrated, a more ambitious goal should be aimed for.

Electronic logic processors such a field-programmable gated arrays (FPGA) or complex programmable logic device (CPLD) are based on arrays of interconnected basic logic units (BLE), depicted in fig. 1, which are composed of a 4-input look-up table (LUT) and a flip-flop.

We study de viability of an architecture for the implementation of this kind of LUT, based on the use of 4-bit optical NOR gates [5].

Architecture

The truth table of a 4-bit LUT is composed by 16 sequential addresses given by the combinations of the possible state of the 4-bit input address. For each of these addresses, a logic value is programmed. Thus, the output of the LUT will be the value stored in the address corresponding to the 4-bit input. Using boolean logic, the operation of a LUT is usually expressed as a sum of AND gates ($\underline{A}\cdot\underline{B}\cdot\underline{D}\cdot\underline{C} + \underline{A}\cdot\underline{B}\cdot\underline{C}\cdot D + \underline{A}\cdot\underline{B}\cdot C\cdot\underline{D} + \ldots$)[1] indicating the input combinations that produce a logical ‘1’ output (0000, 0001, 0010, …). The implementation of these functions could be accomplished using optical AND and NOT gates, but using 2-bit gates implies at least 3 levels of component cascading and a high SOA count, which is undesired.

However, we can take advantage of the 4-bit logic NOR gate that we previously demonstrated using a single SOA [5].

[1] $A\cdot B$ = AND (A,B); $A+B$ = OR(A,B); $\underline{A}$ = NOT (A)

Implementing each NOR gate with a single SOA, and using four additional SOAs, acting as a NOT gate to achieve the inverted address signals (A, B, C, D), a total of 20 SOAs are required for the full implementation of the LUT. For the final OR gate, a direct coupling can be used, as only one address can be active at given time. Finally, the programming itself of the LUT is performed by controlling the bias current of the SOA of each address. If biased, the SOA will act as a NOR gate. If not biased, the SOA will absorb the signals and a logic '0' will be the output for that corresponding address.

Conclusion

We have simulated the behavior of the full LUT at 10 Gb/s using VPI software. Experimental measurements have been carried out on commercial devices and also on Photonic Integrated Circuits. The eye diagram of the output signal of the integrated NOR gate at 25 Gb/s is shown in Fig. 3. Further studies are being done on all-optical flip-flops to assess the possibilities of interconnecting several of these LUTs in more complex optical processing devices.

REFERENCES

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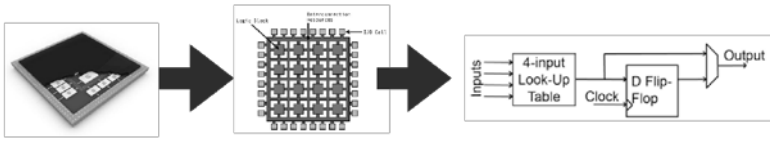

Fig. 1: A logic processor (left) composed of an array of BLEs (center); structure of a BLE (right)

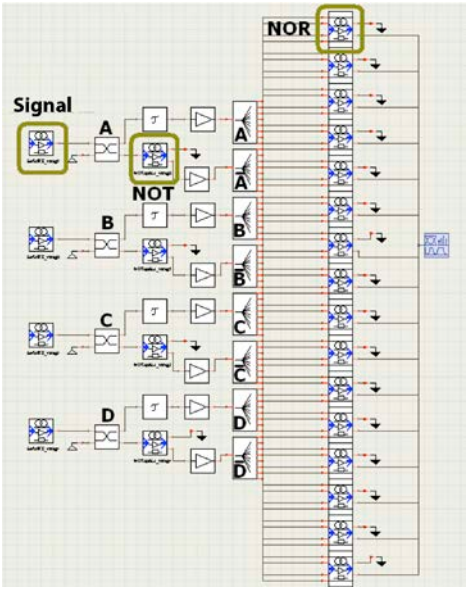

Fig. 2: Simplified simulation schematic for the proposed architecture of the 4-bit LUT.

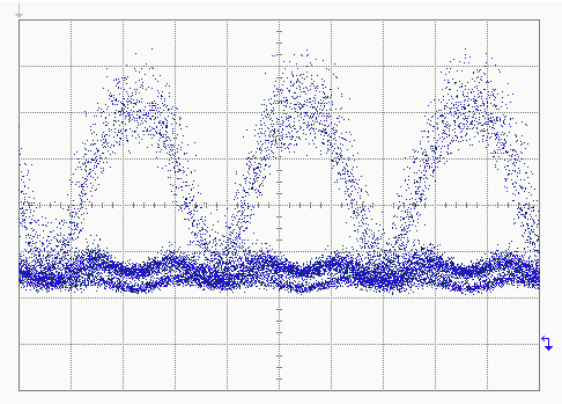

Fig. 3: Eye diagram of the output signal of the integrated NOR gate at 25 Gb/s (RZ amplitude modulation).