Low-power 3V single supply lock-in amplifier

J. Aguirre, N. Medrano, B. Calvo, S. Celma

Group of Electronic Design (GDE) Instituto de Investigación en Ingeniería de Aragón (I3A) Universidad de Zaragoza, Mariano Esquillor s/n, 50018, Zaragoza, Spain. Tel. +34-976761240, Fax +34-976762143, e-mail: jag@unizar.es

Abstract

In extreme high noise level environments, linear filtering is not a suitable processing method and special techniques for accurately extracting sensor signal information should be considered. An interesting possibility are lock-in amplifiers (LIA), which use the phase sensitive detection technique (PSD) to take out the data signal at a specific reference frequency fo while noise signals at frequencies other than fo are rejected and do not affect significantly the measurement. Current commercial LIAs are expensive, heavy and power consuming devices, which preclude their use in portable sensing systems. Thus, this work analyses the possibility of exporting this technique to low-power low-voltage (LPLV) embedded applications. In particular, the aim is to implement a signal conditioning lock-in architecture suitable for 3V single battery-operated wireless sensor nodes. This implies to re-design all the processing elements in single supply -most reported LIAs are designed using dual power supply- and compatible with the power requirements of a wireless sensor network node. Further, looking for a compact LPLV solution, instead of a traditional sinusoidal input, a square wave input is considered, which can be directly obtained from the embedded microcontroller, thus avoiding blocks like a sinusoidal oscillator or function generator. Figure 1 shows the proposed block diagram and a photograph of the implemented device. Experimental results for signals buried in white noise, flicker noise, interference contamination and common-mode voltage contamination confirm the capability of the proposed solution to recover information from signal to noise ratios down to -24 dB with errors below 6% with an average power consumption of only 5 mW in full operation, being able to process signals with frequencies up to 43 kHz, as shown in Figure 2.



Figure 1. (Left) Proposed lock-in amplifier block diagram. (Right) Photograph of the designed device.



Figure 2. (Left) Experimental LIA performance for 26 mV amplitude ideal signal contaminated with 400 mV amplitude white noise. Signals shown, from top to bottom: noise free amplitude, noisy signal, V_{DC1} and V_{DC2}. (Right) With those ideal and noise levels, amplitude recovering error as a function of data signal frequency.