# Improved Precoder Architecture for Duobinary Transceivers

J. Aguirre[1], C. Sánchez-Azqueta[1], E. Guerrero[1], C. Gimeno[2], S. Celma[1]

[1] Grupo de Diseño Electrónico (GDE)
Instituto de Investigación en Ingeniería de Aragón (I3A)
Universidad de Zaragoza, Mariano Esquillor s/n, 50018, Zaragoza, Spain.
Tel. +34-976762707, e-mail: jaq@unizar.es
[2] ICTEAM Institute, Université Catholique de Louvain, Louvain-la-Neuve, Belgium

## Abstract

Duobinary modulation is an attractive baseband modulation scheme for high-speed serial data transmission. This work presents a duobinary transceiver with a new precoder architecture that overcomes the glitch vulnerability of the conventional ones. It has been fabricated in a 0.13-µm PD-SOI CMOS technology and achieves 10 Gbps consuming 37 mW.

## Introduction

The use of techniques to enhance the bandwidth of the communication link, such as equalization or baseband modulation, is mandatory to exceed 1 Gbps in short-range communications. In this frame, duobinary baseband modulation is a very interesting option because it offers the best trade-off between the three most important features of a modulation scheme: data rate, signal to noise ratio (SNR) and power consumption [1]. Duobinary doubles the data rate with respect to standard NRZ modulation by simple and low-power circuitry, without suffering as much SNR penalty as other modulation formats, like 4-PAM.

## Duobinary Precodification

A feasible duobinary transceiver needs two blocks for a correct operation: a precoder in the transmitter and a decoder in the receiver. There are two conventional structures to implement a duobinary precoder in a serialized signal: XOR-based and AND-based precoders [2]. The first one is formed by an XOR gate with a feedback loop through a flip-flop (FF). Its major drawback is that it needs a very precise adjustment of the delay time of the cells to ensure a correct operation. Otherwise, the output produces glitches, which degrades the final result. The second structure is formed by an AND gate in series with a ÷2 frequency divider. It avoids the global feedback loop, which removes the restrictions in the time domain. However, it presents a drawback, which is that the AND gate must be able to work at double data rate than the rest of the cells, since one of its inputs is the clock signal, limiting the maximum data rate of this type of precoders. This work proposes the use of the XOR-based architecture but considering that the output of the system is not the output of the XOR gate, but the output of the Flip Flop. This simple and reliable solution, which has not been reported in the literature, solves the issue of the glitches that is found in the conventional structures and relaxes the constraints in the time domain.

If we define $T_{XOR}$ as the delay in the XOR gate and $T_{D-Q}$ as the delay in the FF, which in turn can be divided into two addends: $T_{D-CLK}$ is the time that passes since the input D experiences a change until the clock flags the sample instant; and $T_{CLK-Q}$ is the delay between the sample instant and the toggle in the output. In the conventional structure, a necessary condition must be accurately achieved: the sum of the delay times of the whole feedback loop must be one bit period $T_b$:

$$T_{XOR} + T_{D-Q} = T_b. \quad (1)$$

If Eq. (1) is not satisfied, the output signal contains glitches that degrade the final result. On the contrary, in the proposed structure, the FF samples the signal once for every bit, so the glitches disappear. To achieve a correct operation, the conditions that must be satisfied are:

$$T_{XOR} + T_{D-Q} < 2\,T_b \quad (2)$$

$$T_{XOR} + T_{CLK-Q} \leq T_b \quad (3)$$

While in the conventional structure the delay times have to be perfectly adjusted, in the proposed structure it is enough to minimize them and, even so, the requirements of the circuits are more flexible than in the conventional case.

# Circuit description

The block diagram of the fabricated transceiver is shown in Fig. 1. The precoder has been implemented with the structure proposed in the previous section. The duobinary decoder has been implemented with a window comparator structure formed by two voltage comparators and an XOR gate. All the cells in this work have been implemented using source coupled logic (SCL) cells, achieving 30% higher data rate in comparison to CMOS static logic [3]. Furthermore, a silicon on insulator (SOI) technological process has been used, achieving a reduction of parasitic capactitances and crosstalk through the substrate.

The channel used in this work consists in a $9^{th}$ order low-pass Bessel filter with 2.2 GHz bandwidth. This filter models a 1-mm diameter 50-m length graded-index plastic optical fiber (GI-POF) achieving an excellent agreement with experimental results.

# Results

The precoder consumes 13.8 mW and the decoder 23.2 mW fed with 1.2 V single supply. The designs are tested for 10 Gbps with a pseudo-random bit sequence of $2^{31}$-1 bits, achieving an excellent energy efficiency of 3.7 pJ/bit. Fig. 2 shows the photograph of the fabricated die while it is tested in a probe station. Fig. 3 shows the eye diagrams of the main parts of the transceiver: the precoder output, signal PRE; the channel output, signal DUO; and the decoder output, signal DEC. A bit error rate (BER) of $10^{-12}$ has been measured for a received power of -14 dBm.

# Conclusion

This work presents a duobinary transceiver fabricated in 0.13 µm PD-SOI CMOS technology. This transceiver uses a new precoder architecture, which overcomes the disadvantages of the other architectures resported in the literature, avoiding the appearance of glichtes and achieving reliable operation. The proposed transceiver reaches 10 Gbps over an electrical equivalent model for 1-mm 50-m GI-POF channel. The full transceiver exhibits a competitive energy efficiency of only 3.7 pJ/bit.

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## REFERENCES

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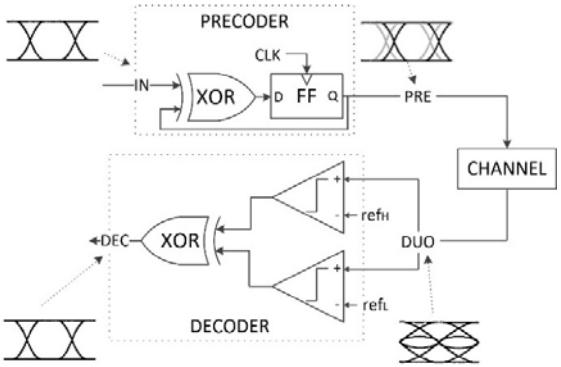


Fig. 1. Block diagram of the proposed duobinary system.

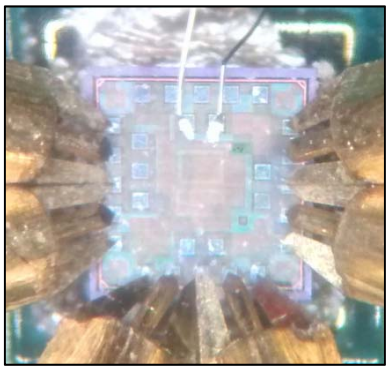

Fig. 2. Photo of the fabricated die and the on-wafer test setup.

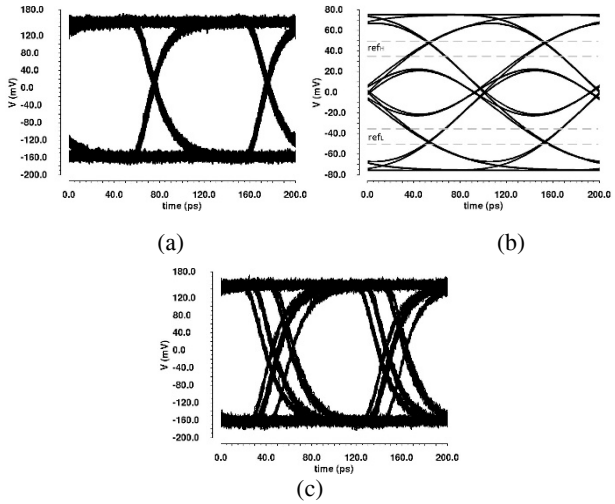


Fig. 3. Eye diagrams for 10 Gbps at (a) precoder output, (b) channel output, (c) decoder output.