A Low-quiescent Current Full on-chip 1.2 V CMOS Low Drop-Out Regulator

Jorge Pérez-Bailón, Belén Calvo, Nicolás Medrano

Grupo de Diseño Electrónico (GDE)
Instituto de Investigación en Ingeniería de Aragón (I3A)
Universidad de Zaragoza, Mariano Esquillor s/n, 50018, Zaragoza, Spain.
Tel. +34-976762707, e-mail: *jorgepb@unizar.es*

Abstract

This paper presents a fully-integrated low-power 0.18 µm CMOS Low-Dropout (LDO) regulator for battery operated portable devices. It provides an accurate 1.2 V output voltage from 3.3 V to 1.3 V input voltages up with only 5.9 µA quiescent current, including an all-MOS 0.4 V reference voltage.

Motivation

Low-Dropout (LDO) regulators are essential blocks in battery-powered portable systems that provide, from the battery input voltage, a stable, noise-free and accurate output voltage V_{out} under variations of the current demanded by load. The current trend in portable applications is towards system-on-chip (SoC) designs, making use of fully integrated CMOS LDOs not requiring an off-chip µF capacitor for stability. Besides, to prolong the battery cycle, operation with low quiescent current is necessary. However, a low quiescent current unavoidably slows the LDO transient responses. Therefore, the design of on-chip capacitor-less regulators requires new compensation schemes and transient enhancement techniques to allow greater integration capability without degrading the performances in terms of regulation, size and power efficiency. To accomplish this goal, several techniques have been proposed that usually involve increasing the chip area and power consumption [1-3].

Proposed LDO

The proposed LDO (Fig. 1) consists of a voltage reference V_{ref}, an error amplifier (EA) driving a PMOS pass transistor between the battery-voltage V_{BAT} and the stable output voltage V_{out}, and a resistive feedback network $R_{fb1} - R_{fb2}$. It has been designed in the low-cost 0.18 µm CMOS process from UMC to provide a 1.2 V output from a 3.3 V battery-compatible input voltage, with a maximum 50 mA load current over a 50 pF load. The all-MOS 0.4 V voltage reference V_{ref} is shown in Fig. 2; it is based on a 2-transistor (2T) voltage reference which uses subthreshold transistors with different V_{TH} levels [4], to accomplish a power-area efficient temperature and supply independent solution (Fig. 3). Resistances R_{fb1} and R_{fb2} in the feedback network are diode-connected PMOS to optimize area. The simplest high-gain single-stage EA suitable for low-voltage operation is used: a folded-cascode, which besides allows cascode compensation (Cc = 6.1 pF) to ensure stability. For transient enhancement, a dynamic biasing method - active only during the transient stages- is adopted based on quasi-floating gates (QFG) M_{QP}-$M_{QN,QN'}$ detection circuits, which require minimal additional hardware. In this way we manage to attain good static performances (Fig. 4) while the transient response is fastened (Fig. 5) without jeopardizing the power consumption (I_q = 5.9 µA) and the complexity of the design (area = 0.04 mm^2).

The LDO main performances are summarized in Table 1 and compared with previous designs with similar specifications [2, 3].

Conclusions

A low quiescent current all-MOS 1.2 V CMOS LDO voltage regulator has been proposed for battery-operated SoC systems, achieving a very competitive trade-off between quiescent current, line and load regulation performance and transient behavior with a compact topology.

REFERENCES

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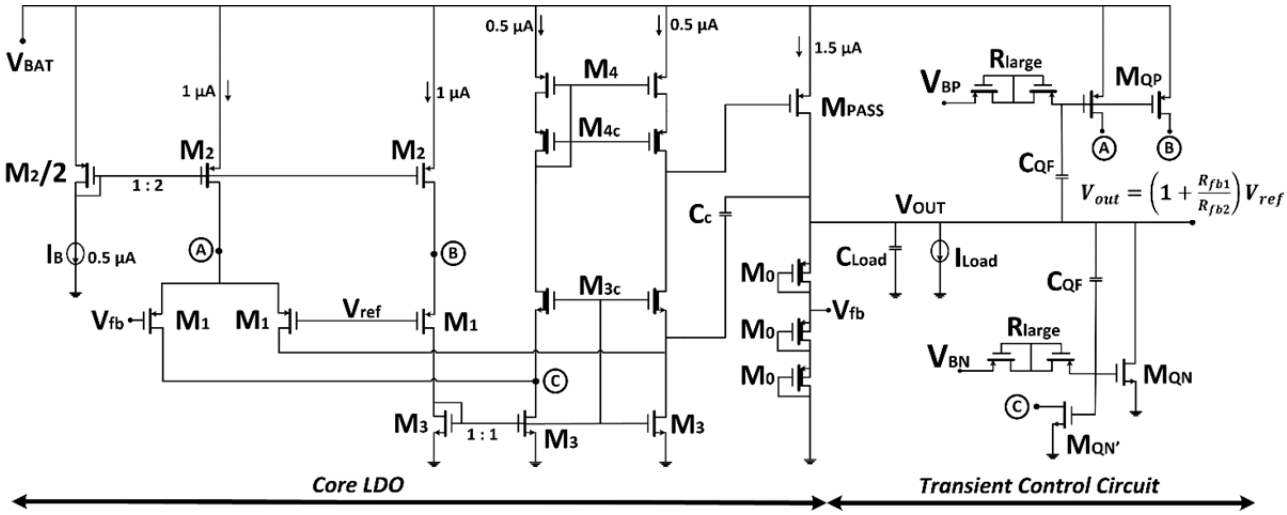

Figure 1: Schematic of the proposed CMOS LDO.

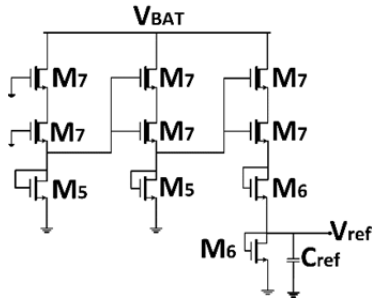

Figure 2: Schematic of the proposed reference voltage.

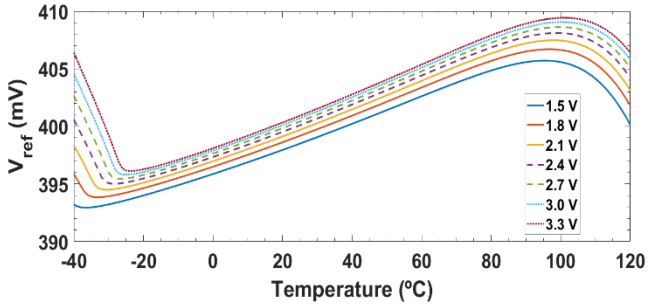

Figure 3: V_{ref} dependence with temperature at different V_{BAT}. 104 ppm/ºC (worst case).

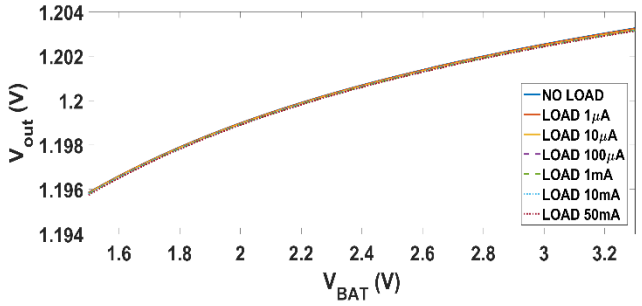

Figure 4: Line regulation for different load currents with desgined 0.4 V V_{ref}.

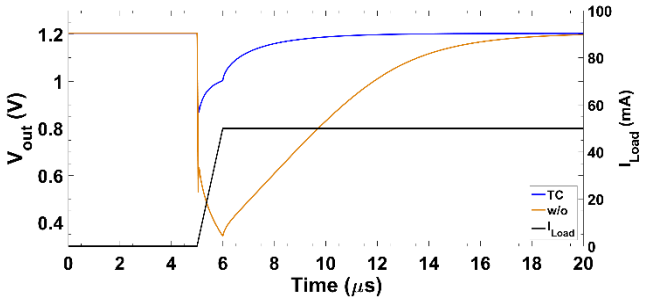

Figure 5: Full load undershoot transition for V_{BAT} = 3.3 V, with and without the transient enhancement circuit.

Table 1. Comparison of CMOS capacitor-less LDO regulators performances.

Parameter	*(ideal V_{ref})**	*(CMOS V_{ref})**	*2011 [2]*	*2016 [3]*
CMOS Technology (µm)	0.18	0.18	0.35	0.35
V_{in} (V)	1.3 – 3.3	1.3 – 3.3	1.642 – 5	3.7
V_{out} (V)	1.2	1.2	1.5	3.25
V_{do} (mV)	120	120	142	300
$I_{Load,max}$ (mA)	50	50	100	50
C_{Load} (pF)	50	50	100	100
I_q (µA)	5.9	5.9	27	26
LNR (mV/V)	0.038	4.10	1.046	-
LDR (mV/mA)	0.002	0.002	0.0752	~2.86
Full load ST (µs)	5.4	5.4	1	0.2 [(b)]

This work, simulation; [(a)] 50 µA – max; [(b)] 0.1mA - max

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