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A Digitally Programmable Active-RC Filter for On-Chip Portable Sensor Applications

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Abstract

An enhanced digital tuning approach for RC-active circuits is presented. Simulations of a 12-bit CMOS second-order filter provide a 11.46-bit effective resolution to linearly control the frequency over three decades with THD < -70 dB. Its low power, 0.5 mW, and low active area, 0.087 mm^2, prove its suitability for on-chip sensing systems.

Motivation

This work is focused on the design of a highly reconfigurable low-power on-chip preconditioning stage to support CMOS impedance and MEM microresonator-based sensors. This requires a wide frequency tuning range -from hundreds of Hz to hundreds of kHz- not achieved so far with current CMOS technologies, further complying with the key constraints of portable systems: compact size and high power efficiency [1-2].

Tunable Filter Implementation

To cover the target frequency range, the most suitable approach is based on RC-active circuits, using core analog cells (typically OpAmps) to achieve a low-voltage low-power compact solution, and incorporating digitally programmable elements to overcome the limited tuning capability of this approach. This work proposes the use of a new CMOS digitally programmable block based on a hybrid current summing/division network (CS/DN, Fig. 1) that, besides, provides linear frequency-to-code dependence. The current summing network (CSN), based on a second generation current conveyor (CCII$^+$), provides the m most significant bits (MSB), while the l least significant bits (LSB) correspond to a current division network (CDN) implemented with a MOS R/2-R ladder. Its input/output current relationship is given by

$$I_{out} = I_{LSB}\left[1 + \sum_{j=0}^{n-1} d_j 2^j\right] = \frac{I_{in}}{2^l}[1 + D(n)] \quad (1)$$

where d_j are the coefficients of the n-bit digital control word $D(n)$.

This CS/DN, with $m = 4$ and $l = 8$, has been used to implement a 12-bit digitally programmable second order KHN universal filter (Fig. 2), fully integrated in a 1.8V-0.18µm CMOS technology. The filter active cell is a specifically designed 2-stage OpAmp (Fig. 3) that features as main performances 95 dB DC gain, rail-to-rail operation, 10 MHz unity gain frequency and 126.5 µW power consumption. The response of the basic programmable active RC-integrator (Fig. 4) with $R = 100$ kΩ, $R_F = 1$ MΩ and $C = 30$ pF shows a characteristic frequency given by

$$f_o = \frac{1}{2\pi C R_{EQ}} = \frac{1}{2\pi CR}\frac{1+D(12)}{256}; \quad R_{EQ} = \frac{256R}{1+D(12)} \quad (2)$$

which linearly ranges from 216 to 887 kHz (4.5% maximum error) with a phase error lower than 0.5º.

For the filter, with HRP resistances $R = 100$ kΩ, $R_1 = R_2 = R_3 = R_F = 50$ kΩ and MIM capacitors $C = 30$ pF, low-pass (v_{LP}), high-pass (v_{HP}), and band-pass (v_{BP}) outputs are attained, characterized by a gain $k = \sqrt{R_1 R_F}/R_2 = 1$, a quality factor $Q = R_3/\sqrt{R_1 R_F} = 1$, and a characteristic frequency f_o given by (2). It occupies 0.087 mm^2 (active area) of which 0.0645 mm^2 is used by capacitors, with a power consumption of 0.5 mW. Fig. 5 shows the digitally controlled low-pass section magnitude response, which varies linearly from 205 Hz ($D = 0$) to 850 kHz ($D = 2816$) preserving Q almost constant (11.46 bits effective resolution). Table I summarizes its main performances and compares them with previous works.

Conclusions

A 1.8V-0.18µm CMOS KHN filter has been presented featuring linear frequency tuning over three decades, with good distortion figures, reduced area and 0.5 mW power consumption.

REFERENCES

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[2]. A. RASEKH, M. S. BAKHTIAR. Design of Low-Power Low-Area Tunable Active RC Filters. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2017. DOI: 10.1109/TCSII.2017.2658635.

Fig. 1. Proposed CS/DN architecture and symbol.

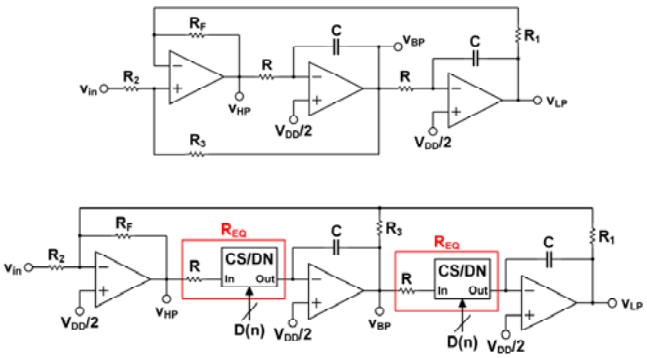
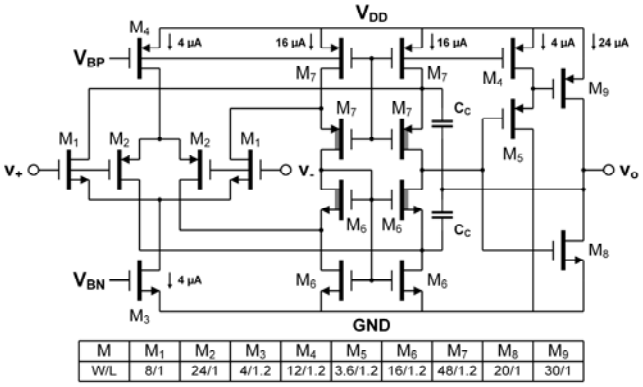


Fig. 2. KHN filter: classical (up) and proposed (down).



M	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
W/L	8/1	24/1	4/1.2	12/1.2	3.6/1.2	16/1.2	48/1.2	20/1	30/1

Fig. 3. OpAmp scheme and transistor sizes in (µm/µm).

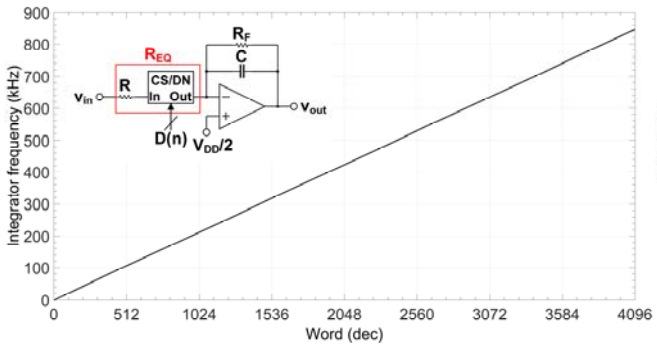


Fig. 4. 12-bit RC-active integrator and its characteristic frequency.

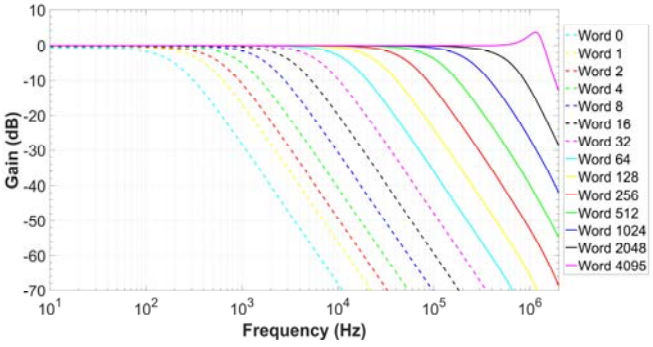


Fig. 5. Digital frequency tunability of the low-pass filter.

TABLE I. KHN FILTER PERFORMANCES AND COMPARISON

Parameter	[1], 2008, meas.	[2], 2017, meas.	This work, 2017, sim.
Operation (Order)	CDN (2^{nd} order)	CSN (4^{th} order)	CS/DN (2^{nd} order)
Technology (Supply)	CMOS 0.35 µm (±1.5 V)	CMOS 0.18 µm (1.8 V)	CMOS 0.18 µm (1.8 V)
Resolution	6 bit, binary code	6 bit, thermometer code	12 bit (11.46 effective bit), binary code
Tuning Range (Step)	300 kHz – 3 MHz (42 kHz)	300 kHz – 1 MHz (100 kHz)	205 Hz – 850 kHz (302 Hz)
Power Consumption	6.9 mW	0.5 mW	0.5 mW
Distortion Levels	THD = -60 dB @ 10 kHz, 1 V_{p-p}	IIP3 = 25 dBm	THD = -70 dB @ 10 kHz, 1.5 V_{p-p}
Input Noise	658 nV/$\sqrt{Hz}$ @ 10 kHz	250 nV/$\sqrt{Hz}$ @ 10 kHz	215.2 nV/$\sqrt{Hz}$ @ 10 kHz
Silicon Area	0.0493 mm^2	0.14 mm^2	0.087 mm^2