A Low Pass Filter With sub-Hz Cutoff Frequencies for a Portable On-Chip Lock-in Microinstrument

Jorge Pérez-Bailón, Belén Calvo, Nicolás Medrano

Grupo de Diseño Electrónico (GDE)
Instituto de Investigación en Ingeniería de Aragón (I3A)
Universidad de Zaragoza, Mariano Esquillor s/n, 50018, Zaragoza, Spain.
Tel. +34-876553257, e-mail: *jorgepb@unizar.es*

Abstract

This paper presents a first-order single-ended fully-integrated Low Pass Filter (LPF) tunable from 114 mHz to 2.5 kHz, designed to conform the output stage of a portable lock-in amplifier requiring f_c = 0.5 Hz, 5 Hz cutoff frequencies. It achieves the two target f_c over a -40 to 120 °C range with a power consumption of 2.7 µW at 1.8 V supply, compact size and dynamic range above 80 dB.

Motivation

LPFs with very low cutoff frequencies (f_c) are key blocks in front-end sensor interfaces, where they serve as pre-conditioning stages to reduce noise and increase resolution over the frequencies of interest, such as in biomedical systems [1], or as DC extractors, placed in the last stage of the readout chain and requiring sub-Hz f_c, such as in lock-in amplifiers (LIA). The latter is the motivation of this study: the design of a LPF constituting the final stage of a CMOS dual-phase LIA (Fig. 1) to be used in a portable on-chip instrument. Most integrated LIAs use off chip resistors and capacitors, keeping the LPF external, because the integration of low f_c filters with low noise and wide linear input range is not trivial, being a real challenge if compact size and low power must be also satisfied.

Proposed LPF

A G_m-C approach (Fig. 2) is adopted to attain a high impedance input node, which makes straightforward the coupling between stages. The core is a mirrored cascode OTA. The input NMOS differential pair remains unaltered, so that the bias point is not moved from its optimum value. The G_m reduction and tuning is done in the output stage, exploiting a cascode current mirror steering technique: the cascode gate voltage V_C is replaced by complementary control voltages $V_{\pm}=V_C \pm V_{gc}$ [2], as shown in Fig. 3, so that output current is split into currents I_A and I_B, each with complimentary gain $\{K_i, (1-K_i), 0 < K_i < 1\}$, adjustable depending on the value of V_{gc}. Output B is the integrator output, and output A is kept at $V_{dd}/2$ to preserve symmetry and assure linear current division.

The LPF has been designed in the 0.18 µm CMOS technology from UMC, with V_{dd} = 1.8 V and V_{cm} = 0.9 V. The capacitor has been set to 50 pF, considered the maximum practical on-chip value. The bias current I_{Bias} is set to 500 nA. The tuning voltage V_{gc} can be varied in a range from 0 to ~200 mV, ensuring a DC gain error below 0.5 dB and a maximum offset of ±1% over a temperature range from -40 to 120ºC. Fig. 4 shows the filter magnitude response at room temperature by steeping V_{gc}: the f_c can be linearly tuned from 2.5 kHz to 114 mHz. For f_c = 0.5, 5 Hz input linear range is 0.13-1.51 V, THD=1%@0.72 mV_{pp} (Fig. 5) and noise 12.8 μV_{rms}, which renders a dynamic range of over 80 dB. The f_c variations over corners and temperature can be adjusted to the target values thanks to the proposed scheme. The main performances are summarized in Table 1 and compared with previous designs with similar specifications [1, 3, 4].

Conclusions

A very low frequency LPF topology has been presented, showing very competitive performances in terms of achievable cut-off frequencies, dynamic range, power consumption and reduced area thanks to the use of a very simple G_m reduction-tuning technique based on current steering current mirrors.

REFERENCES

[1]. R. RIEGER et al. A 230-nW 10-s Time Constant CMOS Integrator for an Adaptive Nerve Signal Amplifier, *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1968-1975, Nov. 2004.

[2]. J. RAMIREZ-ANGULO et al. New Gain Programmable Current Mirrors Based on Current Steering, *IEEE MWSCAS, 2006.*

[3]. P. BRUSCHI et al. A Fully Integrated Single-Ended 1.5-15-Hz Low-Pass Filter With Linear Tuning Law, *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1522-1528, Jul. 2007.

[4]. E. RODRIGUEZ-VILLEGAS et al. A sub-Hertz nanopower low pass filter, *IEEE Trans. Circuits and Systems II: Exp. Briefs*, vol. 58, pp. 351-355, 2011.

This work has been partially supported by TEC2015-65750-R (MINECO/FEDER, UE)

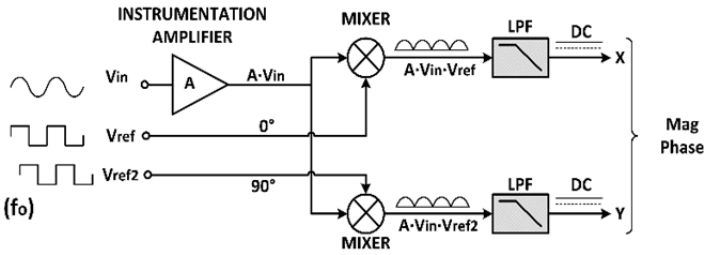

Figure 1: Block diagram of a Dual-Phase Lock-In Amplifier.

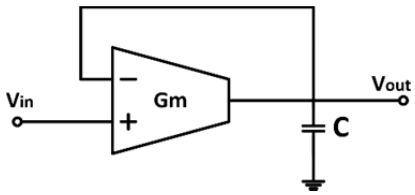

Figure 2: Single-ended basic G_m-C integrator.

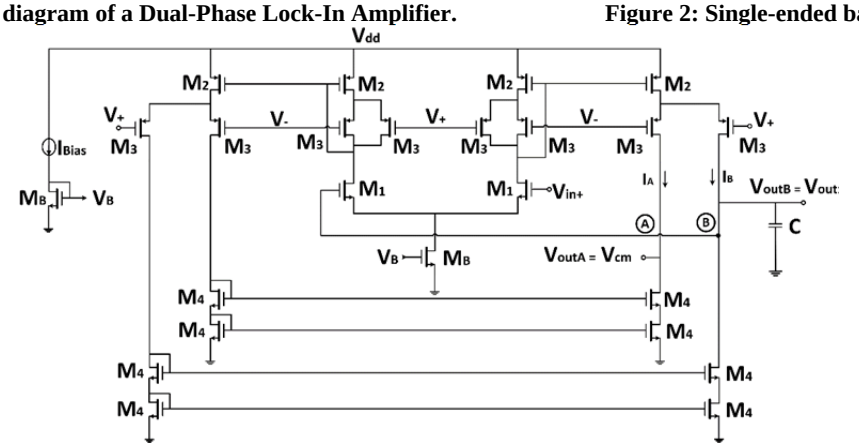

Figure 3: Proposed LPF based on current steering mirrored cascode OTA.

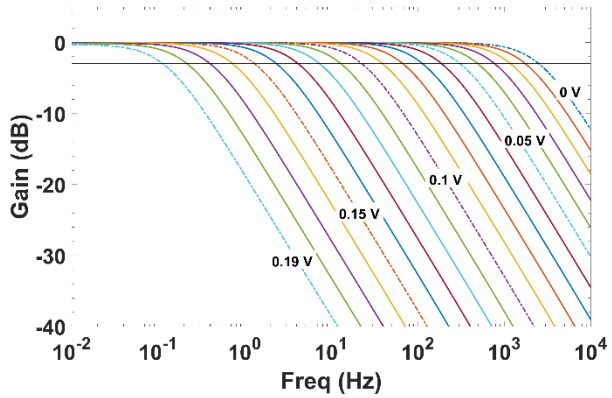

Figure 4: Cut-off frequency tunability, for different V_{gc} values.

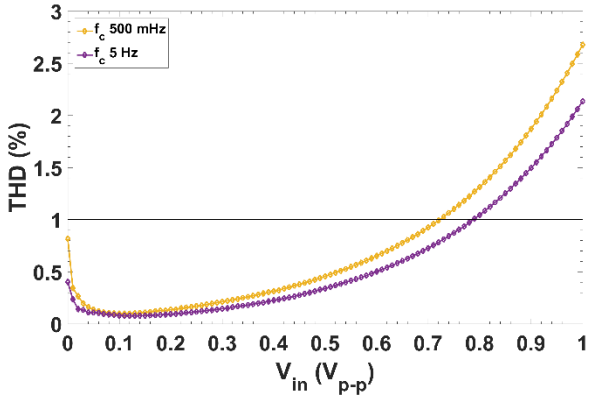

Figure 5: THD vs signal amplitude (pp) for $f_{in} = f_c/5$.

Table 1. LPF performance comparison with similar works.

Parameter	*This work*	*2004 [1]*	*2007 [3]*	*2011 [4]*
Tech. (µm)	0.18	0.8	0.35	0.35
V_{supply} (V)	1.8	±1.5	3.3	1
I_{Total} (µA)	1.5	0.077 + 2.17	50 – 500	0.005
Power (µW)	2.7	0.23 + 6.5 [(b)]	<1650	0.005
C_{Total} (pF)/pole	50	70	52.5	40
Offset	1%	NA	NA	NA
T range (ºC)	-40 – 120	NA	0 - 80	NA
ICMR (V)	0.35 – 1.6	NA-Not Available	0.85 – 2.85	0.4 – 0.55
f_c (Hz)	0.114 – 2.5k	0.1 – 5	1.5 – 15	0.002 – 90
Noise (µV_{rms})	11.3; 12.8[(a)]	NA	NA	32 @ f_c=1 Hz
THD @1% (V_{pp})	0.72; 0.79[(a)] (f_{in}=f_c/5)	NA	1 @ f_c=1 Hz, f_{in}=f_c/5	0.14 @ f_c=f_{in}=1 Hz
Order	1	1	2	1
Area (mm^2)	0.051	0.1 core	0.336	0.07
Dyn.range (dB)	> 80	NA	> 60	64

[(a)] f_c = 0.5;5 Hz; [(b)] 0.23 µA core + 6.5 bias circuitry