

A Fully Differential Variable Gain Amplifier for Portable Impedance Sensing Applications

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Abstract

This paper presents a Variable Gain Amplifier (VGA) designed in a 0.18 μm CMOS process to operate in an impedance sensing interface. Based on a transconductance-transimpedance (TC-TI) approach with intermediate analog-controlled current steering, it exhibits a gain ranging from 5 dB to 38 dB with a constant bandwidth around 318 kHz, a power consumption of 15.5 μW at a 1.8 V supply and an active area of 0.021 mm^2 .

Motivation

Electrical Impedance Spectroscopy (EIS), in which the electrical impedance of a sample under test is evaluated over a certain frequency span, is a powerful sensing technique in a broad range of areas including environmental monitoring, security enhancement, material characterization or the biomedical field [1]. However, despite its versatility, the exploitation of these applications outside specialized laboratories is hindered by the lack of suitable fully integrated electronic interfaces complying with the critical low power and compact size requirements while simultaneously preserving the accuracy and reliability of laboratory equipment.

To extract the magnitude and phase, the simplest hardware-software technique, and thus potentially the most suitable for a CMOS low-voltage low-power (LVLP) implementation, is the Frequency Response Analyzer (EIS-FRA) technique based on quadrature modulators [2], shown in Fig. 1a. The analog preprocessing stage for a typical Mag-Phase read-out channel is a fixed (30 to 50 dB) gain Low Noise Amplifier (LNA) followed by a variable gain amplifier (VGA), which renders further adjustable amplification to optimize signal processing. This work focuses on the design of the VGA, being our design specifications: adjustable 40 dB gain, bandwidth > 100 kHz, to cover most EIS applications, and minimum size and power consumption.

Proposed structure

The proposed VGA relies on a TC-TI approach (Fig. 1b) based on the topology presented in [3], but introducing a current steering technique in the transconductor output stage [4].

The transconductor (Fig. 2a) is a R-linear source degenerated differential pair, using super source follower input transistors which act as voltage buffers. Thus, V_{in} is driven to R terminals, generating the linear signal current $I_{in}=(V_{in+}-V_{in-})/R$, which is conveyed to the output stage through high-swing current mirrors that incorporate cascode current steering. In this way, the overall transconductor output current can be controlled through the cascode gate voltage, so $G_m=\alpha/R$, with $0\leq\alpha\leq 1$.

The TI-stage (Fig. 2b), is made of two identical class-AB transresistance amplifiers set in a differential arrangement. Resistance R_f yields the output voltage, being the overall gain given by $A_v=\alpha R_f/R$, while C_f is used for compensation. Both R and R_f are linear passive elements, to optimize linearity and insensibilize the gain to PVT variations.

This VGA has been designed in the 0.18 μm CMOS technology from TSMC, with a 1.8 V voltage supply and a bias current of 0.5 μA using a class-AB topology to optimize power (achieved through a quasi floating C_{bat} and R_{large} gate). The layout is shown in Fig. 3. It provides a variable gain ranging from 5 dB to 38.5 dB (Fig. 4), preserving an almost constant bandwidth of 318 kHz. Total power consumption is 15.5 μW , and active area is 0.021 mm^2 .

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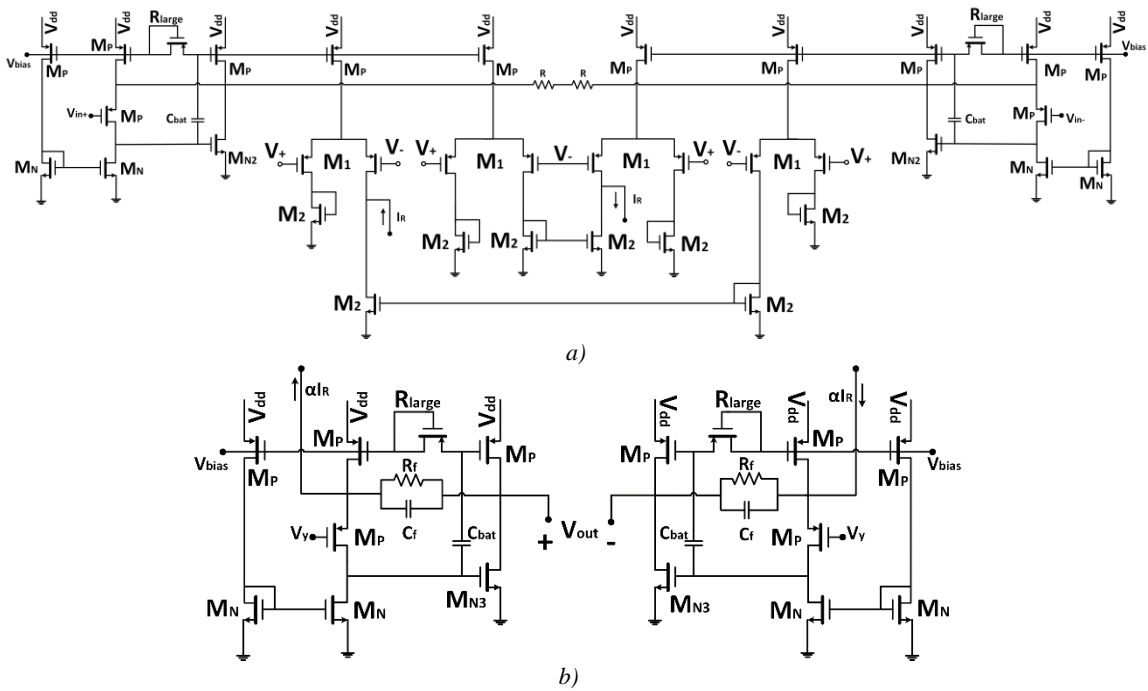
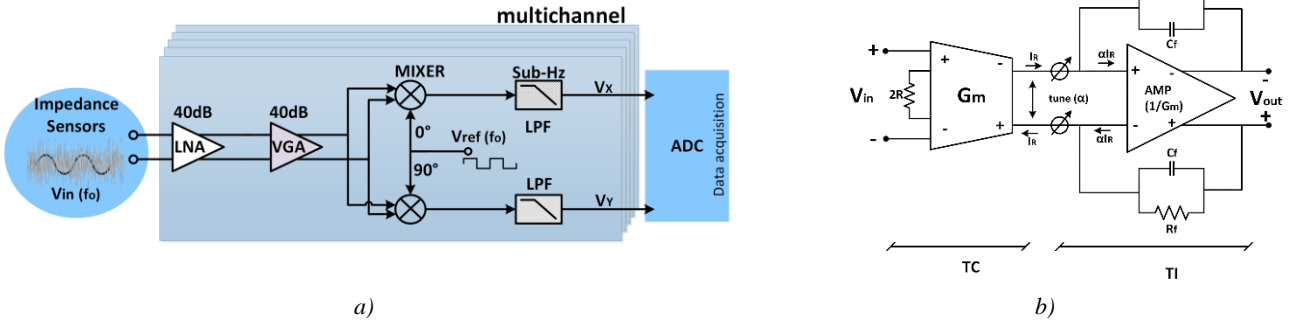


Fig. 2. Schematic view of the proposed VGA: a) TC and b) TI.

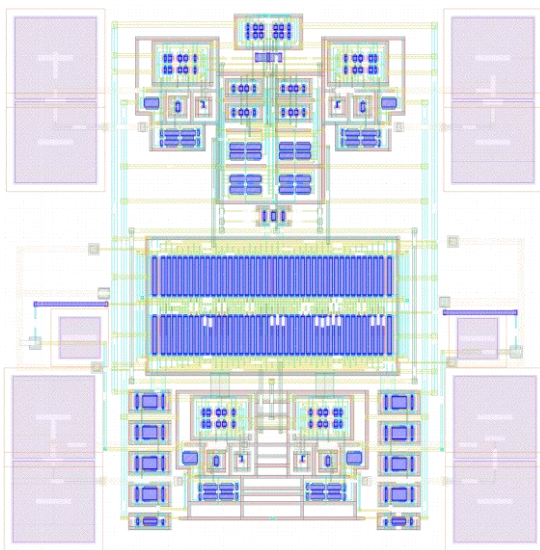


Fig. 3. Layout view of the complete VGA structure. Size: 144x145 μm^2

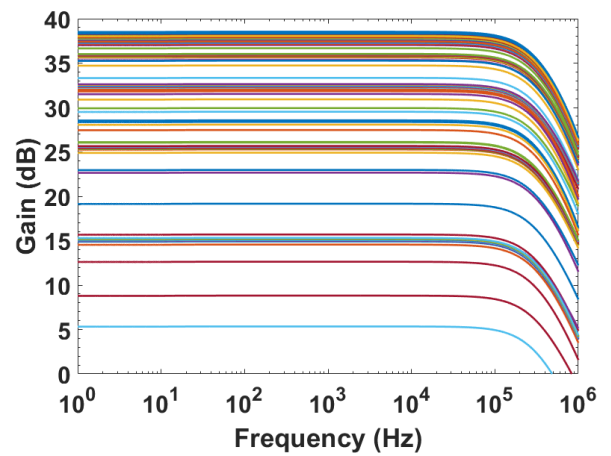


Fig. 4. Gain variation over tuning.