Laser driver design in 65-nm CMOS technology for IFoF optical links

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Abstract

Broadband mobile networks have experimented an accelerated growth in the passed five decades culminating this development with 5G networks. This evolution demands an efficient and not expensive solution for optical-wireless front-end. Thus, information delivered by mobile stations is repeated over a Distributed Antenna System (DAS), where Remote Antenna Unit (RAU) integer optical and wireless modules. A non-linear response from light source means a major problem for an analog signal in comparison with digital one. The main problem with non linearity is signal dispersion giving as result alteration of signal shape form. In this direction there are some options from IC electronic design to interact with optical source, first the use of a linear drive circuit that delivers a certain amount of electric current for a voltage input signal, the second option is the use of pre-distortion or post-distortion electronic blocks to guarantee a lineal response from optical source. This work supposes a first approach and design of a linear laser driver in 65-nm CMOS technology that includes layout design.

Technological Requeriments

The scheme for uplink stablishes some requirements for the block before VCSEL (vertical-cavity surface-emitting laser) or any other inbuilding light source employed to transmit a modulated analog signal represented by a certain range of optical power. A laser driver provides to VCSEL an adequate bias level in addition to an optimal coupling of impedances due to the fact that input impedance of VCSEL is 50 Ω.

On the other hand, is convenient to achieve a good performance with the laser without any control loop stage, this means that linear laser driver desig, consider AC, DC and transient analysis for open loop. Nevertheless, a control loop is needed for practical implementation, where temperature and age can alterate output response of light source (Säckinger 2005).

The structure proposed in this work is based in a degenerated differential pair, where a current mirror provide a linear characteristic for a stable operating point and a wide dynamic range for an input voltage (Ahmad et al. 2017). The laser driver block (LD) in RAU is showed in Figure 1.

Design Constraints

The EDA (Electronic Design Automation) software available at Electronic Design Group (GDE) is Cadence, with PDK (Process Design Kits) of the main foundries. Laser driver is built with n-MOS transistors setting biasing point and common mode at half of value of supply voltage (1.2 V). One of main constraints is set output impedance to 50 Ω, if the design uses resistors at drain terminal there are two possibilities, one is to reach a high gain and output impedance comparable with drain resistance; another is to get a low output impedance and low output gain.

To overcome the limitations described above two differential pair are designed, first stage with high gain and second one with output impedance of 50 Ω. In these conditions, the biasing of two stages compromises DC response and is desirable bias the second one with output of first. Simulation presents adequate results for different analysis, with all transistors working in saturation and a good linear response, with an enough dynamic range of 500 mV in linear region. Further, a bandwidth above 100 MHz has been obtained, which is enough for our IFoF (Intermediate Frequency over Fiber) application.

Laser Driver Integration

Once simulations results are successful, the next step after schematic design is layout generation for TSMC

65-nm CMOS technology. This process has an important trade-off among physical connectivity, silicon area and parasitic capacitances at transistor devices and metal paths. Before fabrication, the foundry requires Design Rule Check (DRC) validation and schematic versus layout correspondence. The extraction of all devices generate a list of all parasitic capacitances, this could modify the frequency response and other characteristics, so a strict validation at physical level before sending design layout to foundry is mandatory. A more graphical view from layout is presented in Figure 2, the dimensions of LD are 81.1 µm by 68 µm.

The research to deploy wireless communications systems demands practical alternatives to repeat modulated analog signals propagated by mobile base stations (BS) under the scheme of a unique system that integrates wireless and optical communications.

Characterization

The workflow for test and measure of IC blocks consist of static and dynamic measuraments, that includes temperature response variation, S parameters, bandwidth at half-point power and transient response to validate signal distortion (Varonen et al. 2008). At this moment, laser driver IC is ready to characterize in laboratory, this task requires a specific printed circuit board (PCB) design, to solve measurement issues given for an incorrect manipulation of test and equipment measurament, derived from reduced size of ICs.

Blocks Integration

One of objetives of research is the RAU integration on a SiP (System in a Package) where all design, manufactured ICs are enclosed in a chip package (Paredes et al. 2020).

Conclusions

The new emerging wireless technologies are more conciencious of an inminent integration of wireless and optical communications through utilization of RoF technologies. In this work, a new scheme of laser driver for IFoF has been proposed. Intermediate frequency over fiber is consolidating as a promising option and the proposal of design and integration in a simple chip of all blocks of a RAU is a good alternative considering the low power consumption, low cost of manufacturing, reliable CMOS integration and good performance in terms of linearity and frequency response.

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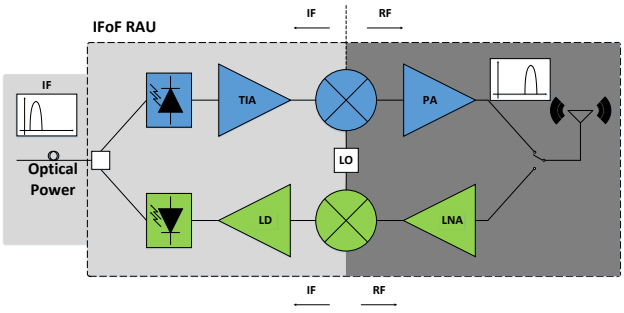

Fig. 1. IFoF RAU scheme and spectral representation

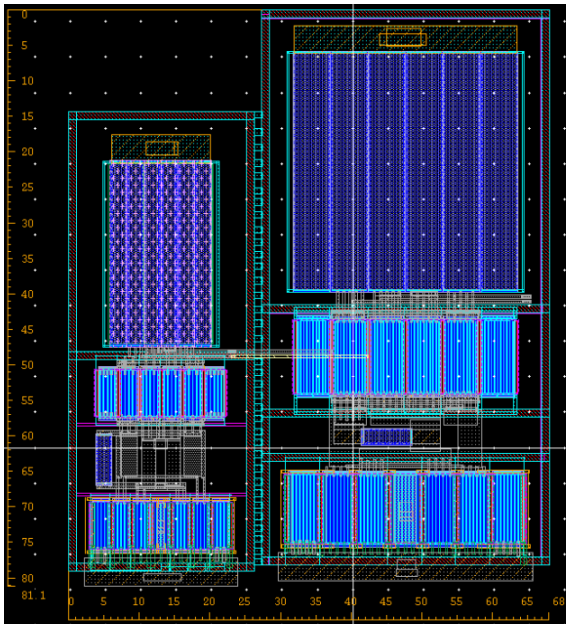

Fig. 2. Laser driver layout