X JORNADA DE JÓVENES INVESTIGADORES DEL I3A

Laser driver design in 65-nm CMOS technology for IFoF optical links

Diego F. Paredes-Páliz[1], Francisco Aznar[2], Antonio D. Martínez-Pérez[1], Santiago Celma[1]

[1] Electronic Design Group (GDE -I3A) - Universidad de Zaragoza

[2] Electronic Design Group (GDE -I3A) - Centro Universitario de la Defensa Zaragoza

dparedes@unizar.es

Objective: Design a linear laser driver at 65-nm CMOS technology

Design Parameters

- Output impedance: 50 ohms
- Dynamic range, quite enough to modulate a VCSEL

Design Modifications

- Two differential pair in cascade configuration
- 1st Stage: Amplification, 2nd Stage: Coupling

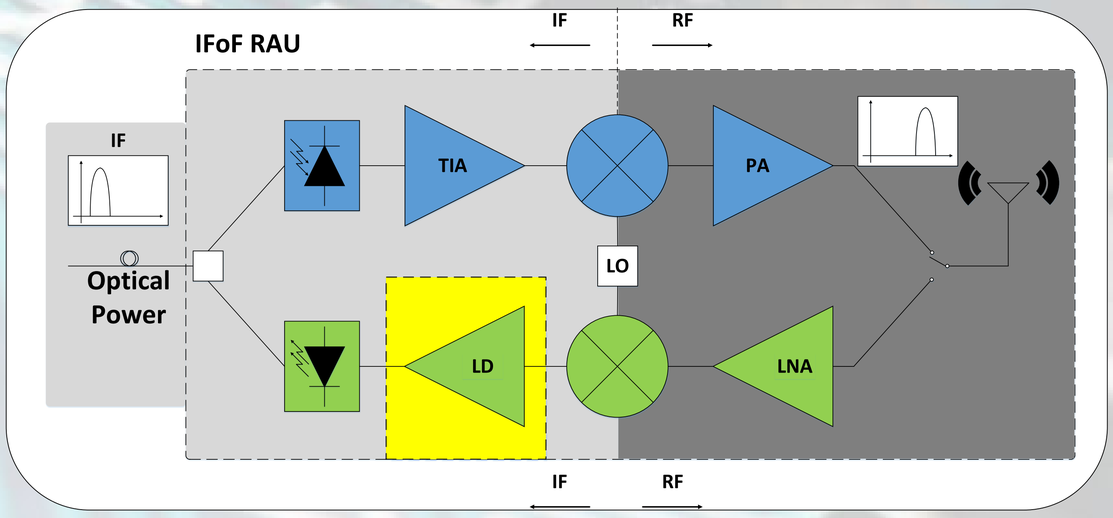
Design Methodology

Motivation

- Broadband mobile networks are the future, like 5G.
- Remote Anntena Unit (RAU) integer Optical and Wireless modules.
- Non-linear response from light source generate signal distortion.
- To avoid distortion a practical solution is the use of a linear drive circuit.
- This work supposes a first approach and design of a linear laser driver (LD) in 65-nm CMOS technology, that includes layout design.

Technological Requirements

- Input impedance of VCSEL is 50 Ω.
- It is convenient to achieve a good performance, including AC, DC and transient simulations.
- In yellow is illustrated the block designed and simulated in Cadence, using process design kits (PDK) for 65-nm.

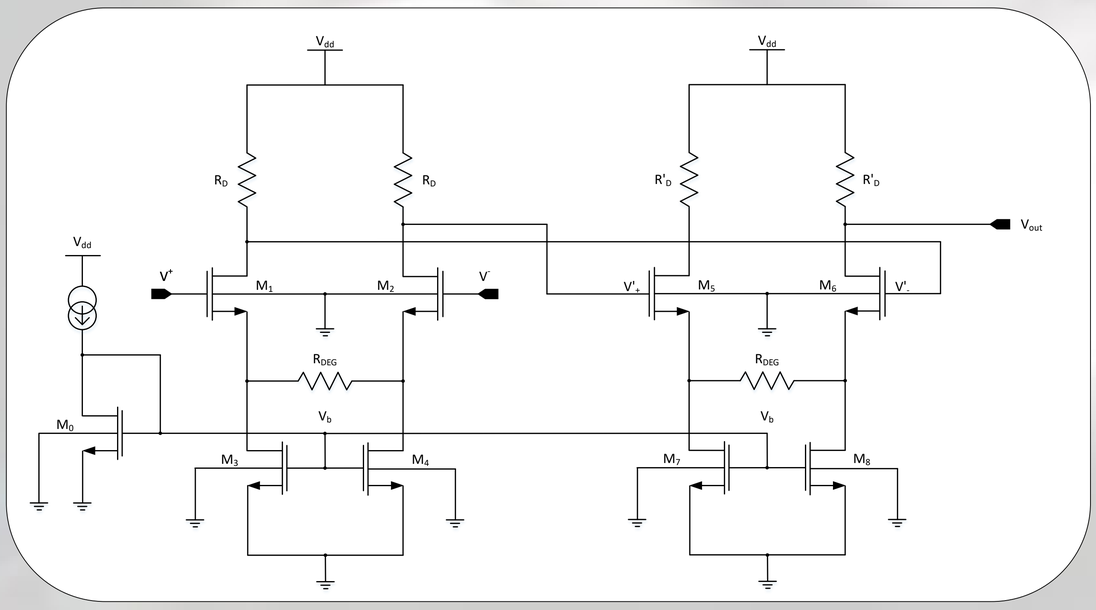


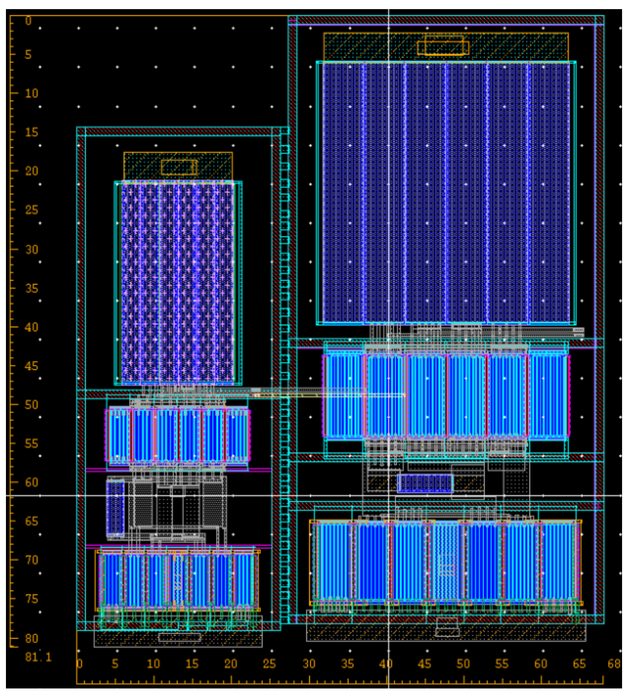
Design Constraints

- Laser driver is built with n-MOS transistors, biasing at common mode point at half of supply voltage (1.2 V).
- Two differential pair are designed, first stage with high gain and second one with output impedance of 50 Ω.
- Simulation presents adequate results with all transistors working in saturation and a good linear response.

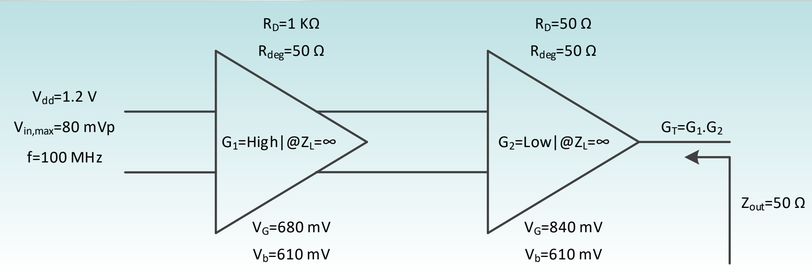
Laser Driver Integration

- After schematic design, follow layout generation for TSMC 65-nm CMOS technology.
- This process has an important trade-off among physical connectivity, silicon area and parasitic capacitances at transistor devices and metal paths.
- A more graphical view from layout is presented below, the dimensions of LD are 81 µm by 68 µm.





Results



Future Work

- Design and integration in a simple chip of all blocks of a RAU to obtain low power consumption, low cost of manufacturing, reliable CMOS integration and good linearity performance.