CMOS design of a phase shifter for 5G/6G active antenna arrays

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Abstract

This paper presents the design of a phase shifter operating over the 18-27 GHz frequency range. The phase shifter is digitally programmable using a 65 nm CMOS process. Schematic simulation results provide an RMS value at 24 GHz of 3.5º for the phase and of 0.76 dB for the gain.

Introduction

Antenna arrays allow the transmission or reception of an electromagnetic wave in a particular direction by controlling the phase of the signal in each antenna. This is possible due to the action of beamformer chips, that vary the phase of the signal through a digital word, eliminating the need to orientate the antennas mechanically. Owing to the high directionality of the beam, interference with other signals is reduced, focusing the signal on the desired targets or users. Consequently, the coverage range and quality of the communication link are increased. These are improvements sought by the new generation of wireless communication systems (5G/6G) and satellite communications (SATCOM) [1].

Hybrid beamforming happens to be the most advantageous topology, as it does not require a complete receiver chain for each antenna and allows working with multiple beams [2]. Hence, the vector-modulator based phase shifter used in this work will be implemented in the receiver path of a hybrid architecture antenna, focusing on the design of the programmable gain amplifier and a power combiner [3].

Proposed Topology

In this active phase shifter topology, a quadrature signal generator (QSG) provides two orthogonal signals (I/Q) which are weighed independently by two programmable gain amplifiers (PGAs), as shown in Fig. 1. Each PGA has a certain gain, we will call A_r the gain of the PGA that weighs the in-phase signal (I) and A_j the gain of the PGA that weighs the quadrature signal (Q). These gains are programmable by a 4-bit word and depend on the number of on/off amplification stages in each PGA. The ideal phase shift can be calculated as $\phi=tan^{-1}(A_j/A_r)$. The signals coming from two different pairs of PGAs are combined using a power combiner.

Quadrature Signal Generator

Achieving quadrature signals with no voltage losses is an essential step in producing the phase shift in signals. The architecture proposed uses an LCR all-pass filter to create two differential signals in quadrature, which has proven to be advantageous compared to other options such as polyphase filters [4].

Programmable Gain Amplifier

The 4-bit digitally programmable PGAs are composed of four blocks (B and C marked in blue) with three switchable cascode structures in parallel and four dummy cascode structures (A and D marked in green), as shown in Fig. 2. The gain of each PGA depends on the amount of current flowing through it, which is regulated by the number of active stages. Current will flow through a cascode structure when a V_{dd} voltage is applied to the upper transistor. The stages A and D use dummy transistors to maintain the total number of on transistors connected to the input and to the output constant, respectively. Consequently, the variations of the input and output impedances between different configurations are minimized.

Power Combiner

The power combiner is the next stage after the PGAs. The signals coming from two different antennas are fed into the structure shown in Fig. 3 [3]. In this work, a phase shifter for a single antenna is designed so only half of this structure (M1 and M2 transistors) will be used. The purpose of including the combiner in the design, is to reproduce the load effect at the PGA output.

Results

The values chosen for the final design are: $R = 65\ \Omega$, $L = 323$ pH , $C = 575$ fF for the LCR based QSG

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elements, $L_0 = 375$ pH, $C_0 = 150$ fF for the elements at the output of the PGA. All the transistors in the PGA have the same length: $L = 60$ nm and the width of the upper transistors in the cascode structure is $W_1 = 9$ µm and for the lower transistors $W_2 = 2.6$ µm, except for the D transistors which are half as wide (W_1 = 4.5 µm, W_2 = 1.3 µm). At the power combiner all transistors have the same dimensions W/L=85 µm/60 nm and L_1=375 pH and C_1=300 fF [5].

It can be seen in Fig. 4 that the phase results are kept constant through the operation range for each configuration, with phase RMS errors lower than 8º and a minimum of 3.5º for 24 GHz, the target frequency of our design. The gains achieved at 24 GHz, ranging from 28.7 dB to 30.06 dB, are high which is important in a receiver and the RMS error is of 0.76 dB, as it can be seen from Fig. 5.

Conclusion

In this paper a programmable phase shifter consisting of an LCR based QSG, two 4-bit digitally programmable gain amplifiers PGA(I) and PGA(Q), and a power combiner, have been designed. Simulation results show that the dummy transistors have managed to reduce the RMS errors in the amplitude and phase of the I/Q signals by keeping input and output impedances constant through different configurations.

The simulation results have been obtained with an RMS error of 3.5º in phase and 0.76 dB in gain at 24 GHz. It has also been confirmed that the different phase states are maintained constant in the K-band frequency range.

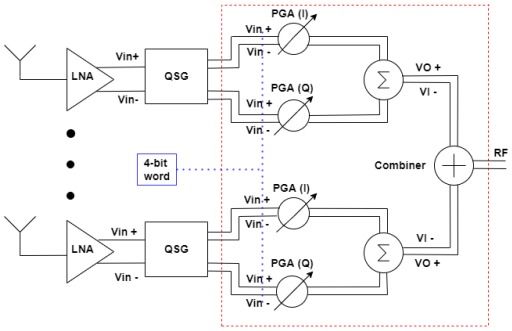

Fig. 1. Block diagram of a hybrid beamforming based receiver. This work will focus on the design of the elements inside the red square: a 4-bit programmable gain amplifier and a power combiner.

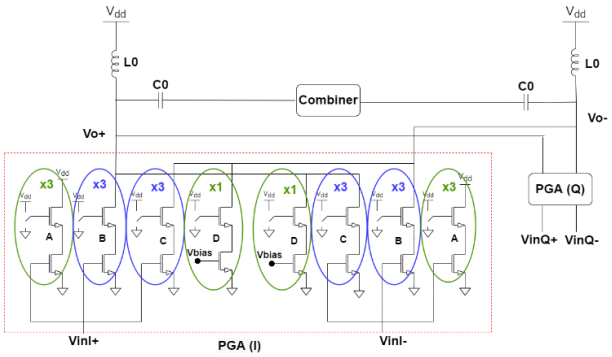

Fig. 2. PGA topology. The structure of an in phase programmable gain amplifier, PGA(I), is ilustrated inside the red squared box.

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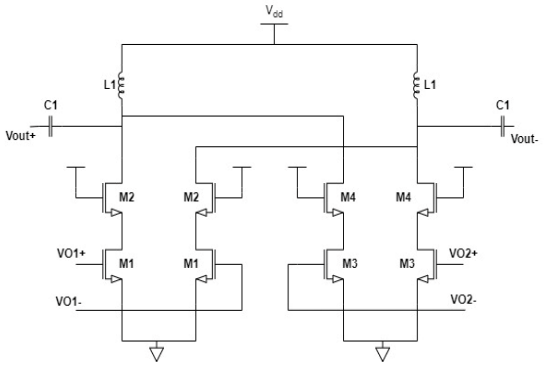

Fig. 3. Topology of the power combiner.

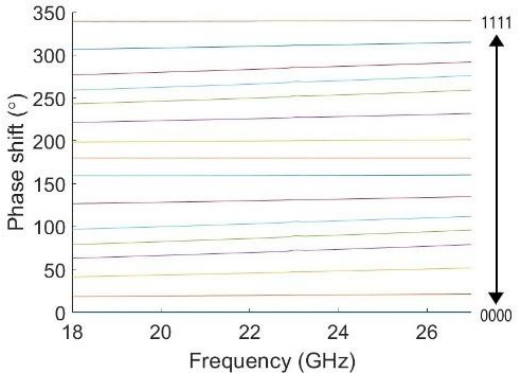

Fig. 4. Phase shifts in a frequency band from 18 to 27 GHz.

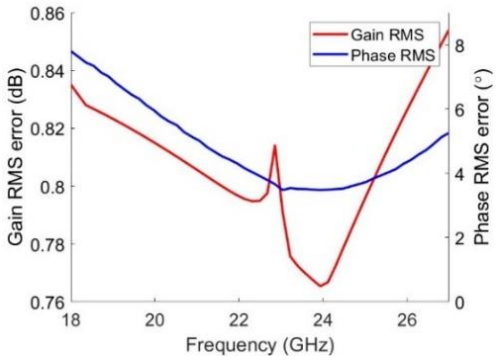

Fig. 5. Phase and gain RMS errors in a frequency band from 18 GHz to 27 GHz.