Design of an active a 5- bit digitally programmable phase shifter for hybrid antenna beamformers

Uxua Esteban Eraso[1], Carlos Sánchez Azqueta[1], Concepción Aldea Chagoyen[1]
Santiago Celma Pueyo[1]

[1] Grupo de Diseño Electrónico (GDE)
Instituto de Investigación en Ingeniería de Aragón (I3A)
Universidad de Zaragoza, Mariano Esquillor s/n, 50018, Zaragoza, Spain.
Tel. +34-976762707, e-mail: uesteban@unizar.es

Abstract

This paper presents the design of a new 5-bit digitally programmable phase shifter using CMOS technology of 65 nm, for its use in hybrid antenna beamformers opperating at the part of the K-band destinated to SATCOM communications. Simulation results are compared with previously reported alternatives.

Introduction

Phased array antennas are essential parts in satellite communications (SATCOM), allowing the radiation patern to be ellectronically directed (beamforming) and to work with multiple beams simultaneously. Beamforming requires adjusting the phase of each of the radiant elements. Therefore, phase shifters become key components in this type of active antenna [1].

Proposed Topology

The topology proposed in this work for the phase shifter involves two building blocks: a quadrature signal generator and a variable gain amplifier (VGA). To generate the cuadrature signal, a new quadrature all-pass differential filter (QAF) is proposed (Figure 1). It is based on the orthogonal phase shift created in RLC resonators [2]. To avoid amplitude errors in the I/Q signals, a mid-stage of common source transistors (one in each I/Q differential path) is used between the QAF and the VGA.

Then, using two 5-bit digitally progammable VGAs, each component of the I/Q signal is weighed independently [3,4]. As shown in Figure 2, each VGA is made up of six blocks (A, B and C) of six NMOS transistors and two blocks (D) of two NMOS transistors. The idea is to drive the desired portion of the current to the output through transistors B and C, while the remaining part is deviated by dummy transistors A and D. Dummy transistors allow to keep constant the total number of transistors switched on conected with each input and each output. This way, the variations of the input and outout impedance between different configurations are minimized and, hence, the phase and gain errors decrease.

Results

The values chosen for the implementation are: $R = 95\ \Omega$, $L = 600$ pH (Q = 17.2 @ 19.5 GHz), $C = 570$ fF, $L_0 = 260$ pH (Q = 21.0 @ 19.5 GHz). For the VGA transistors the dimensioning has been $W/L = 2\ \mu m/60$ nm, whereas the size of the transistors of the source common intermediate stage is $W\ /\ L$ = 16 µm ⁄ 60 nm (not shown). Figure 3 shows the phase shifts obtained for a frequency of 19.5 GHz. It can be seen that for a weighed combination of the in-phase and quadrature signals, the desired phase states are obtained with an RMS error of 3.55º in phase and 0.78 dB in gain.

It has also been verified that the results obtained are maintained in a wide frequency range around the working frequency, from 17 GHz to 22 GHz. In this range, RMS phase errors are lower than 7.00º, and RMS gain errors are lower than 0.90 dB (Figure 4). Table I shows that these resuls are better than those obtained in [2] and [5]. It has also been obtained good S-parameters S_{11} and S_{22}, and better lineality (+ 0.3 dBm of P1dB in relation to [5]) and lower power consumption (- 16% in relation to [5]).

Conclusions

This work presents the design of a phase shifter using a QAF to generate the in-phase and cuadrature signals and two 5-bit controllable VGAs to weigh them. The mean feature of this design are the dummy transistors, which allow to maintain the value of the input and output impedances between different configurations and, consequently, improved linearity and reduced RMS errors are obtained. Simulation results have been achieved with an RMS phase error of 3.87º and an RMS gain error of 0.80 dB at 19.5 GHz. It has also been verified that the different

phase steps are mantained over a wide frequency range, from 17 GHz to 22 GHz.

Acknowledgments

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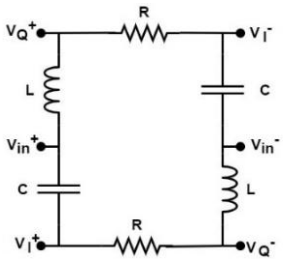

Figure 1. Quadrature all-pass filter topology.

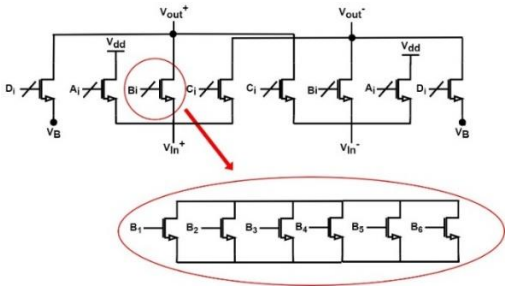

Figure 2. Voltage gain amplifier topology.

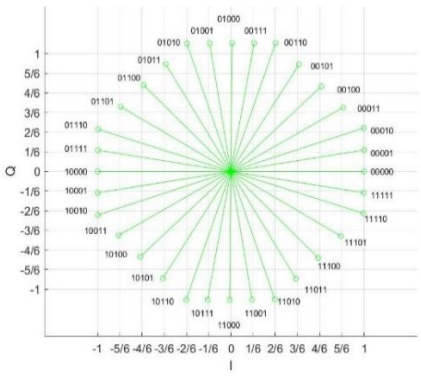

Figure 3. Phase shifts obtained at 19.5 GHz.

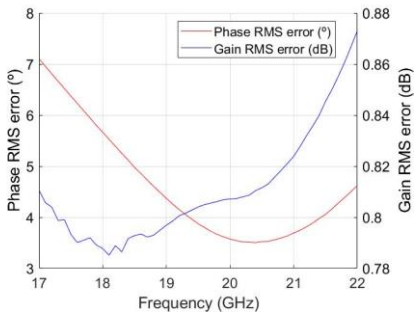

Figure 4. Phase and gain RMS errors.

Table 1. Comparision table.

	Freq. (GHz) / Resolution	Technology (nm) /Supply (V)	$\Delta\phi_{RMS}$ (°)	ΔA_{RMS} (dB)	S_{11} (dB)	S_{22} (dB)	Input P1dB (dBm)	Consumption (mW)
This work	17 - 22 / 5-bits	CMOS (65) / 1.2	3.5 – 7.1	0.78 – 0.87	< -10 @ 17-22 GHz	< -6 @18.7 - 20.5 GHz	-0.5 ± 0.3 @ 19.5 GHz	9.78 @ 19.5 GHz
[2]	50 - 68 / 4-bits	CMOS (65) / 1.5	4 - 12	0.8 – 1.0	<-10 @ 59 - 67 GHz*	< -5 @ 57 - 64 GHz*	-16 @ 60 GHz*	19.5 @ 60 GHz*
[5]	15 - 26 / 4-bits	CMOS (130) / 1.5	6.5 - 13	< 2.1	< -10 @16.8 - 26 GHz	< -10 @ 17-26 GHz	-0.8 ± 1.1 @ 24 GHz	11.7 @ 24 GHz

* Simulations done with LNA and a part of a combiner.