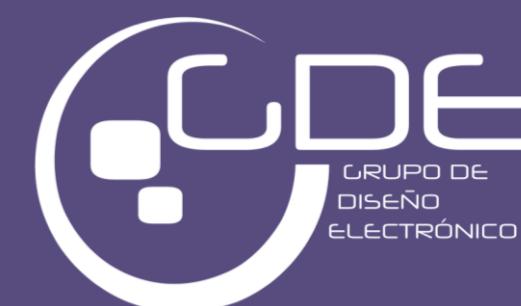


# CMOS design of a phase shifter for 5G/6G active antenna arrays

Carolina del Río Bueno, Uxua Esteban Eraso, Carlos Sánchez Azqueta y Santiago Celma Pueyo

Grupo de Diseño Electrónico (GDE -I3A) - Universidad de Zaragoza

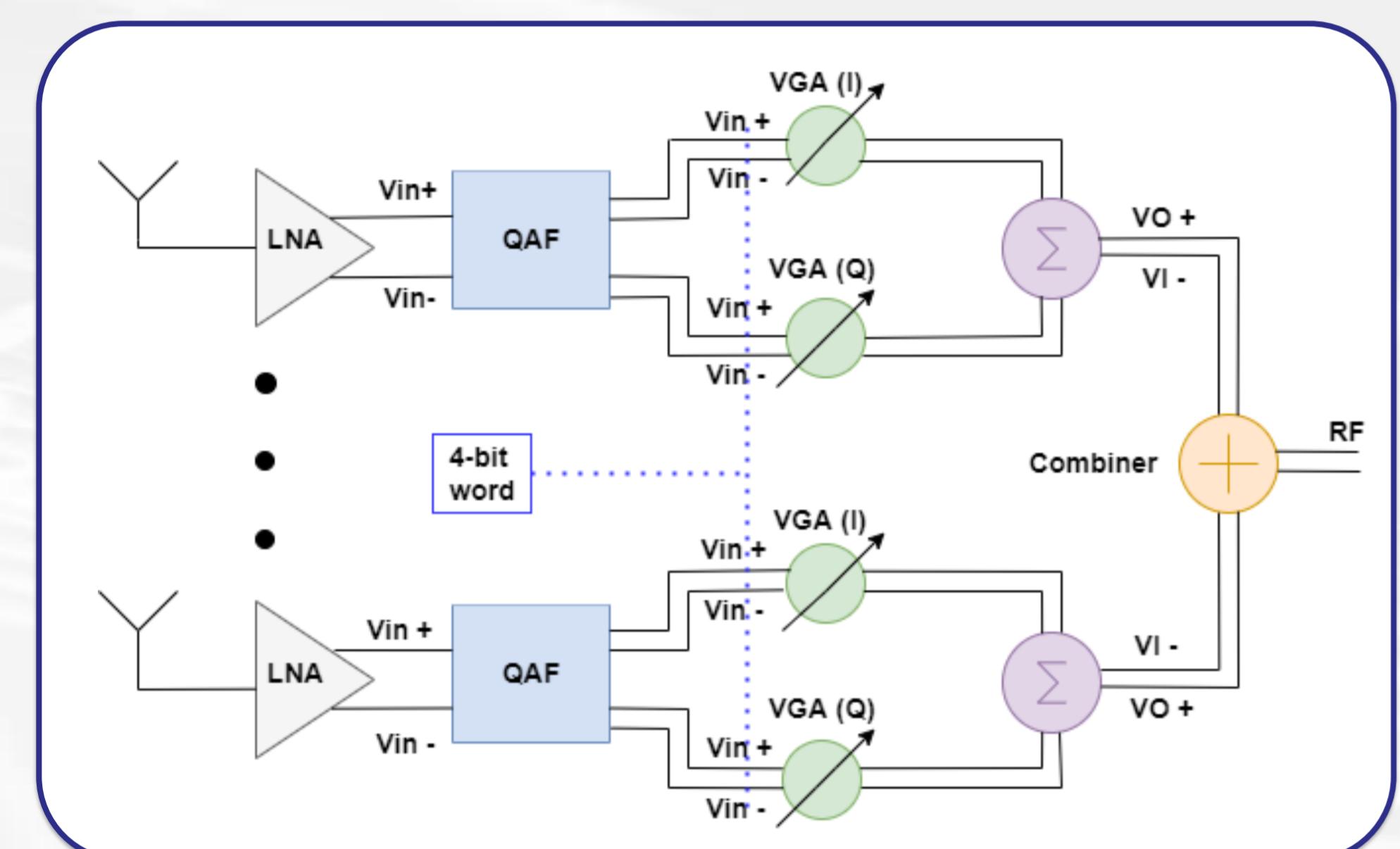
[gde@unizar.es](mailto:gde@unizar.es)



- |               |   |  |
|---------------|---|--|
| <b>K-band</b> | <ul style="list-style-type: none"> <li>✓ Wider bandwidth available</li> <li>✓ Allows the use of <u>antenna arrays</u></li> <li>✓ Higher data transfer velocity</li> <li>✗ Higher attenuation of the signal</li> </ul> | <ul style="list-style-type: none"> <li>✓ Lower interference with undesired signals</li> <li>✓ Electrical steering</li> <li>✓ Cheaper and less power consuming</li> </ul> |
|---------------|---|--|

## Topology

### Phase shifter conceptual scheme:



➤ **Quadrature All-Pass Filter (QAF):**

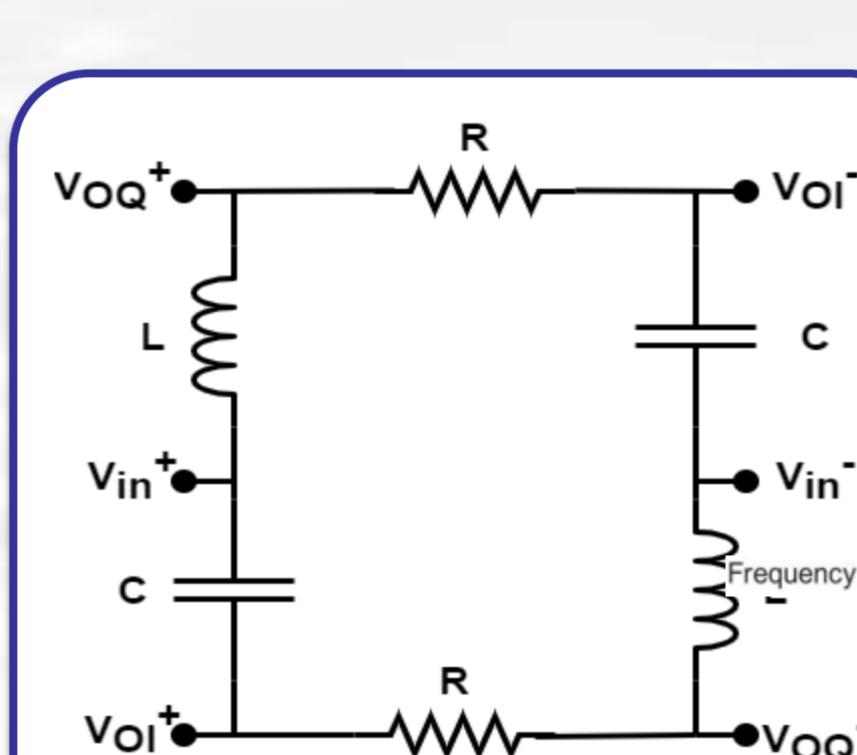
Generates in-phase and quadrature signals

➤ **Variable Gain Amplifier (VGA):**

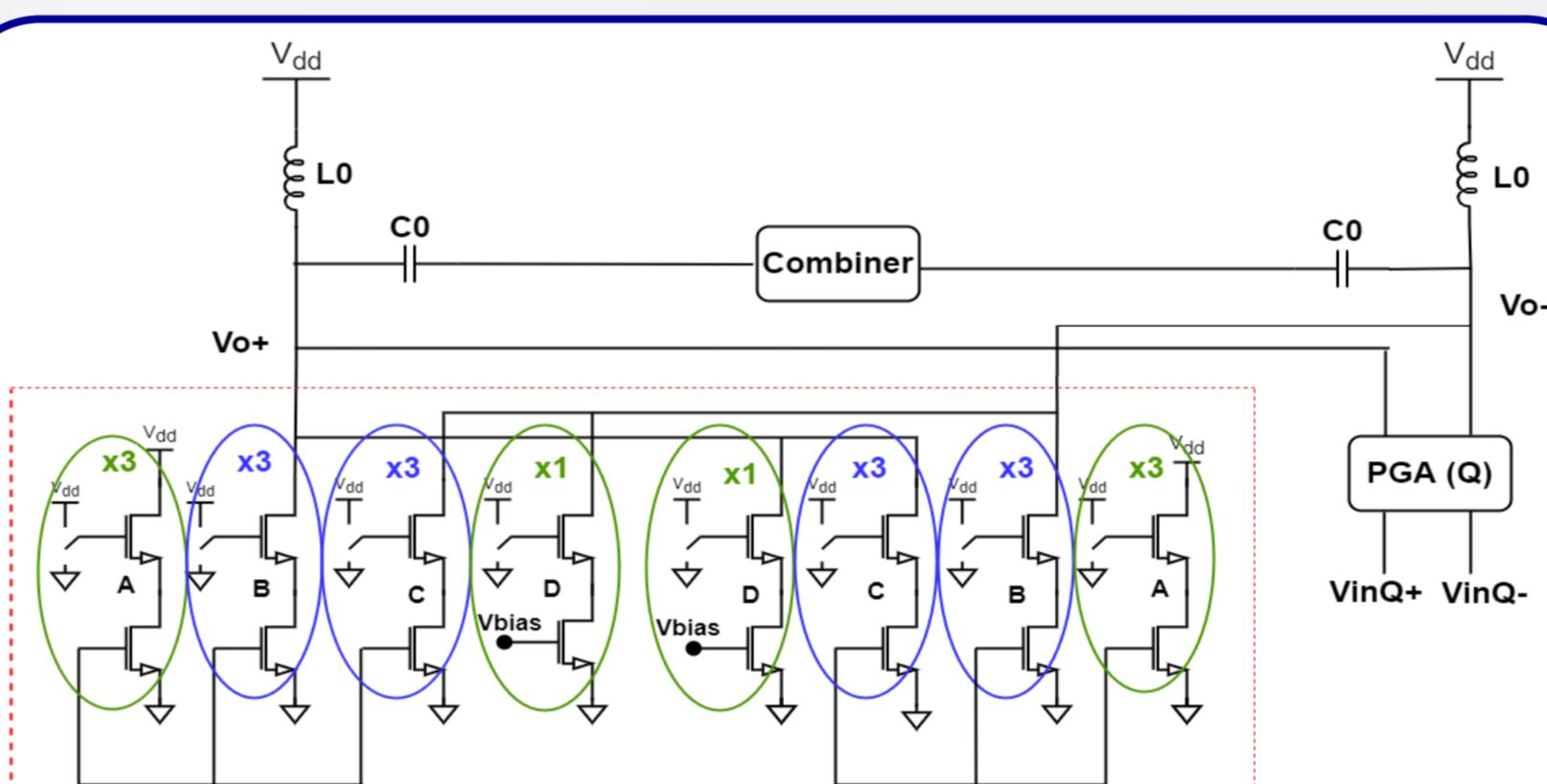
In-phase and quadrature signals weighed by digitally 4-bit programmable cascade VGAs

➤ **Power Combiner:**

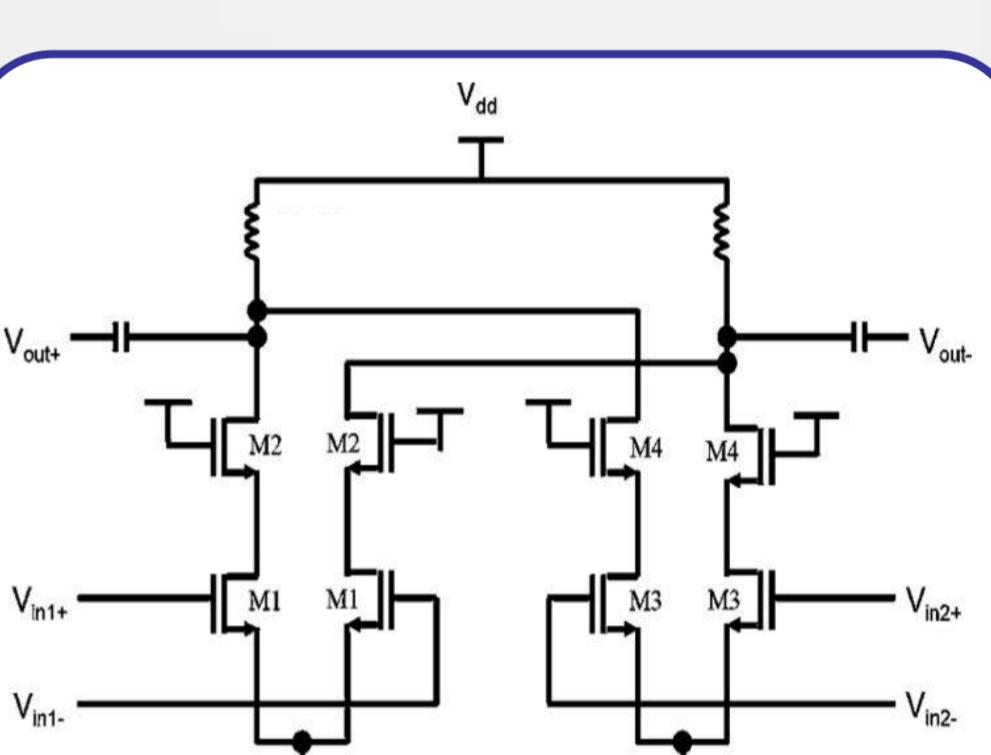
Combines signals coming from different antennas



QAF



VGAs



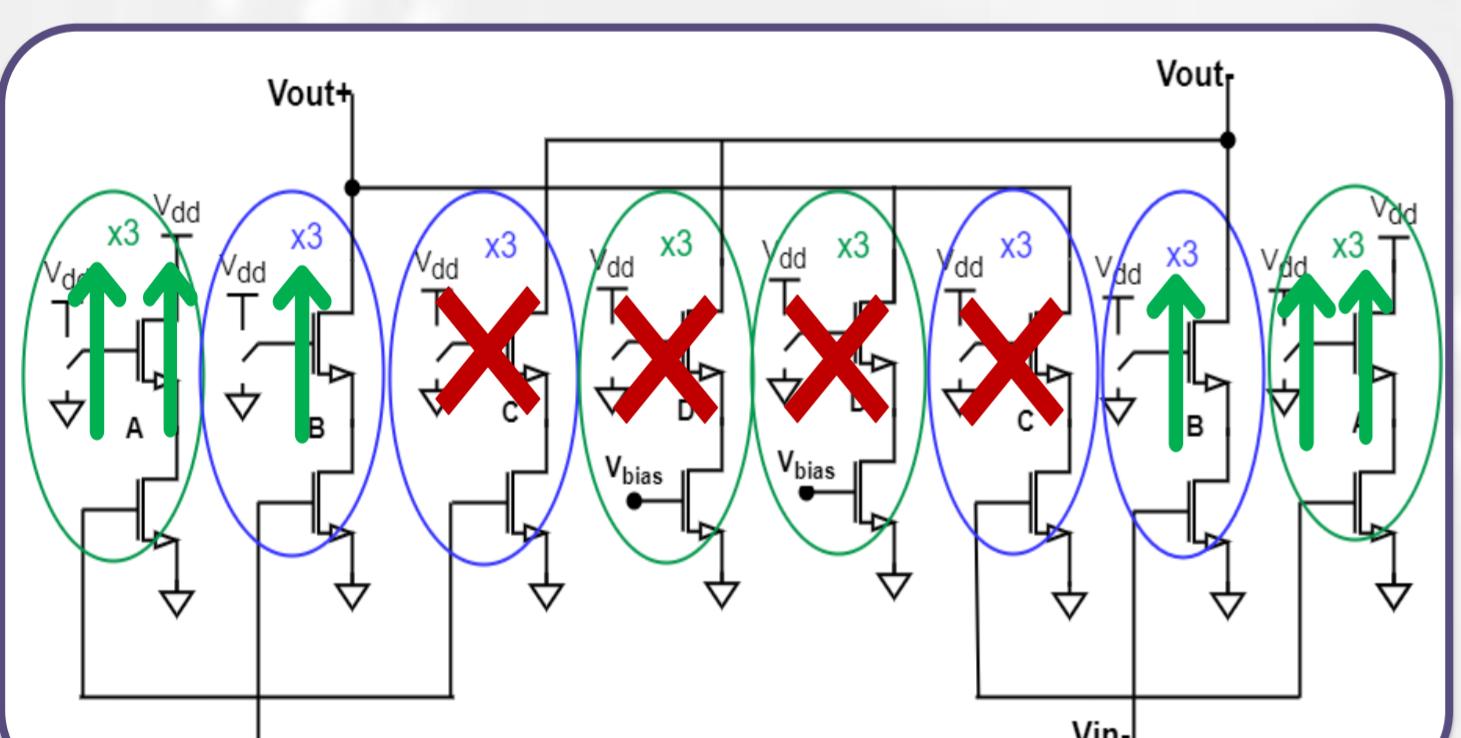
Power Combiner

## Operation of a phase shifter

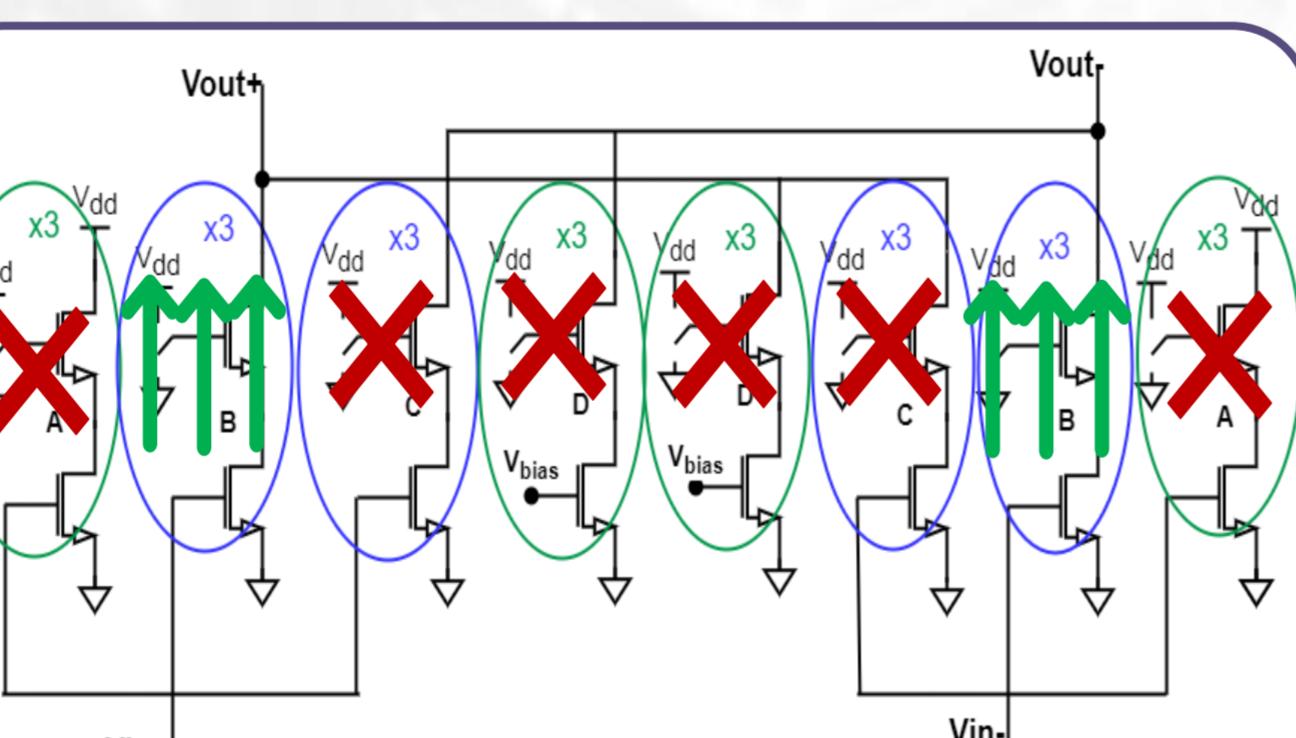
$$\phi = \text{atan}(A_j/A_r)$$

$$\text{Gain} = \sqrt{A_j^2 + A_r^2}$$

VGA (I)



VGA (Q)

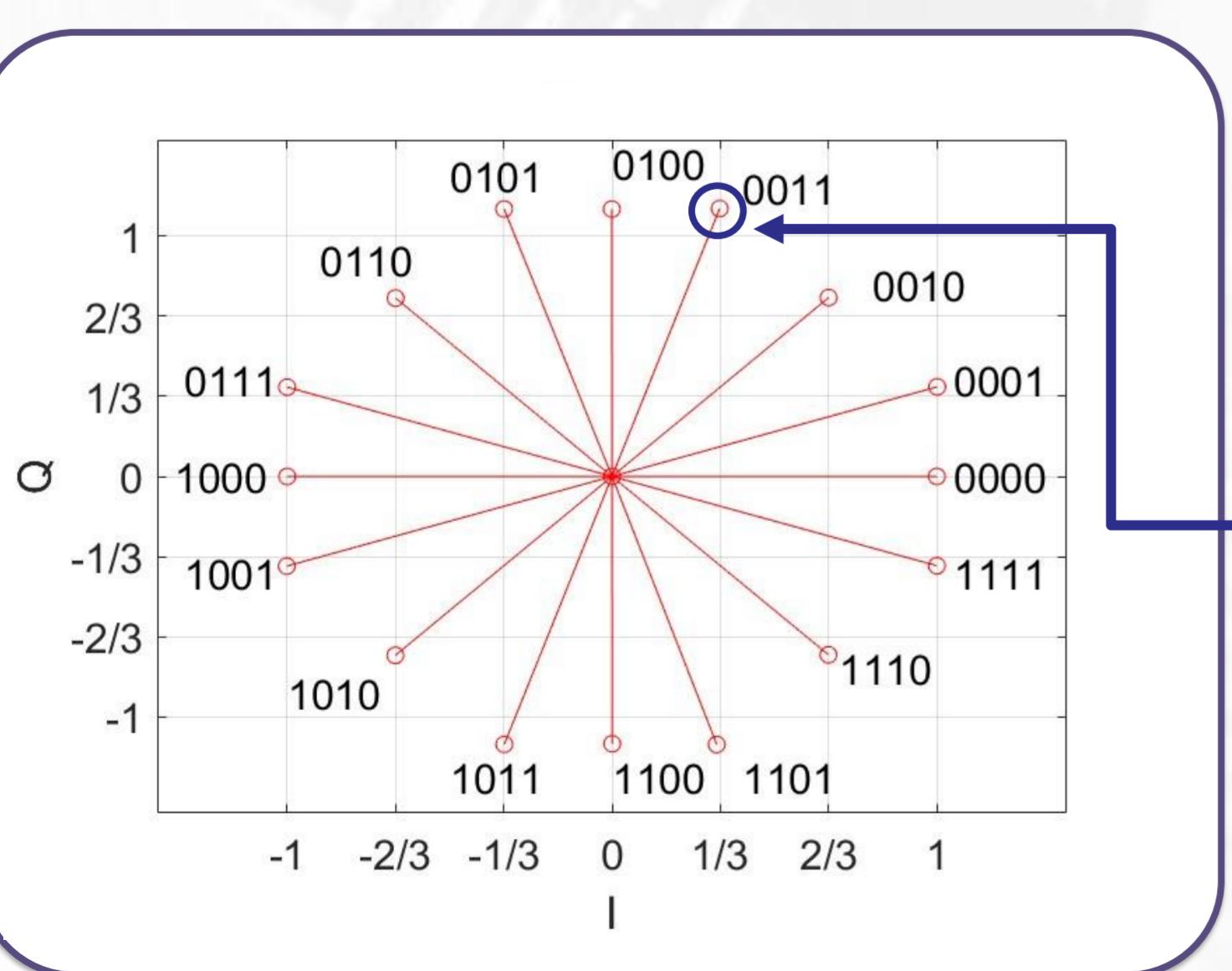


$$A_r = +1/3$$

$$A_j = +1$$

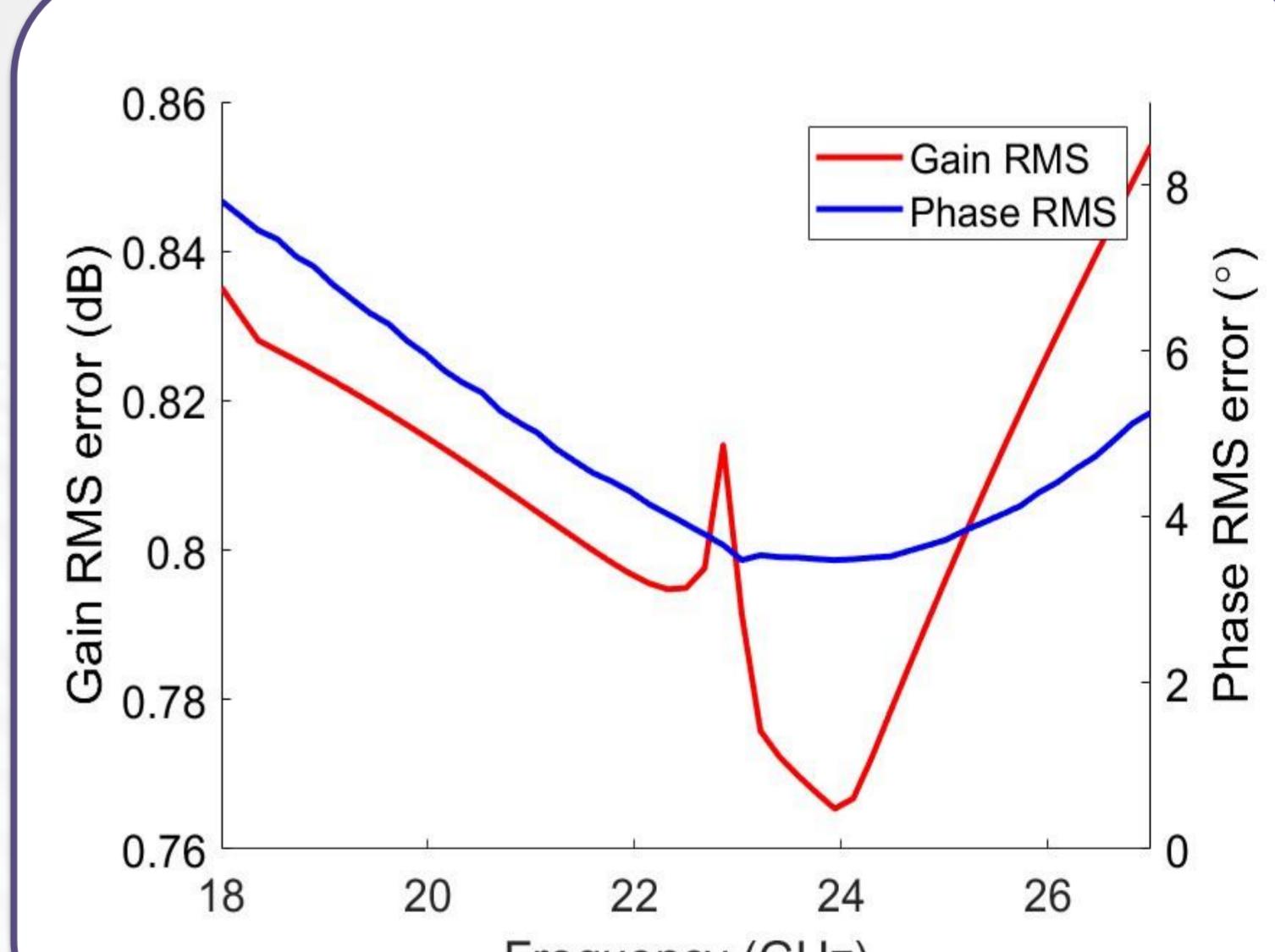
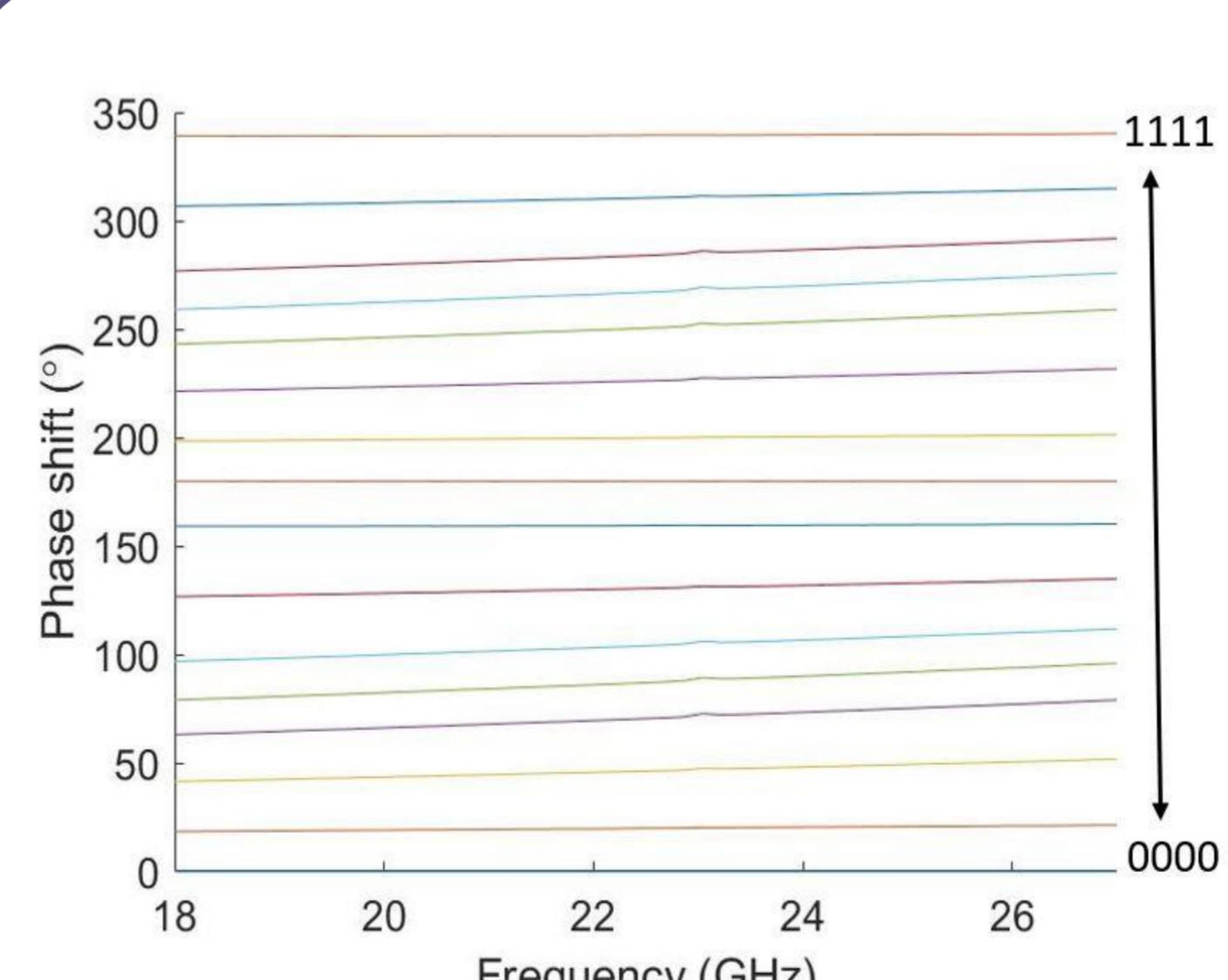
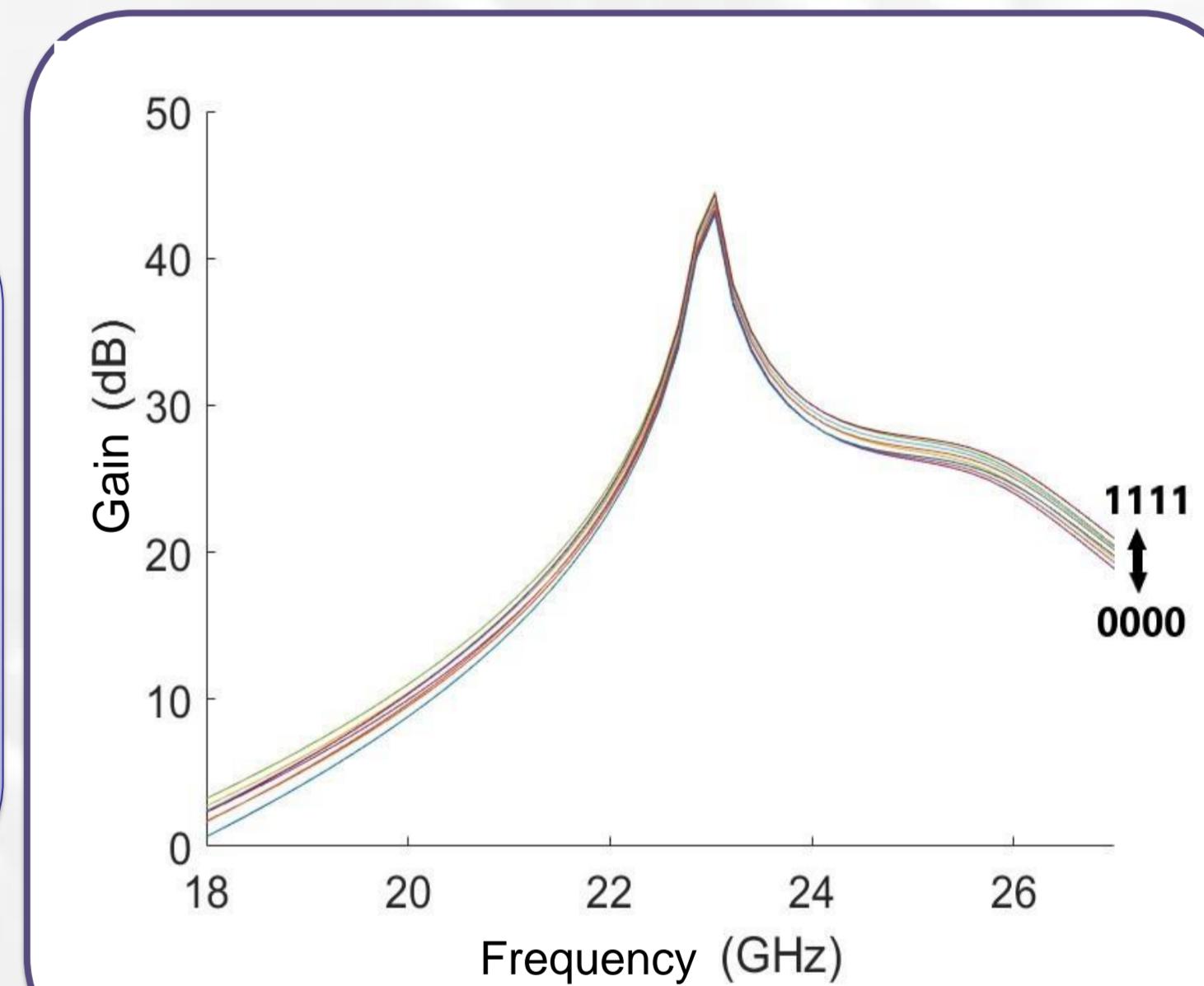
$$A_j/A_r = +3$$

$$\phi = 67.5^\circ$$



## Results

- Frequency: 18-27 GHz
- Technology: CMOS 65 nm
- $\Delta\phi_{RMS}$  ( $^\circ$ ): <8°
- $\Delta A_{RMS}$  (dB): <0.86
- Gain (dB): 28.7-30.06 @ 24 GHz



## Conclusions

- The 4-bit phase shifter produces the desired phase shift according to the control word.
- This phase states are kept constant in the K-band frequency range.
- Dummy transistors reduce the RMS errors by keeping the input and output impedances constant.