A New Multi-Rate Clock and Data Recovery Circuit

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Abstract

A new bit rate adaptive clock and data recovery circuit able to operate in a range from 3.125 Mb/s to 2.5 Gb/s is presented in this work. It is designed in a standard CMOS technology, fed with a single supply voltage of 1.8 V and has a maximum power consumption of 140 mW.

Introduction

In the characterization of digital communication systems, different types of communication signal analyzers are employed to obtain the design parameters such as bit error rate (BER) [1]; some of them require a source of timing synchronization, whereas others need at their inputs a conditioned replica of the output data of the device under test (DUT), as illustrated in Fig. 1.

In the past, communication analyzers were typically designed to test and measure DUTs targeting at most only a few standards and the clock signal used for BER measurements and data synchronization could be either taken from the pattern generator or supplied by the DUT itself. This has changed over time and nowadays, with the arise of many different serial communication standards, a major versatility is required for test equipment to be useful in a laboratory. This has been overcome by either incorporating an internal clock and data recovery (CDR) circuit or by using an external clock signal. In either case, the CDR circuit has the task of extracting the clock reference signal to be used for the signal analyzer as the trigger directly from the received data.

Most of the proposed CDR circuits in the literature are designed to operate in a limited range of data rates, which limits their versatility when are used in instrumentation equipment, where the goal is to characterize different types of DUTs in a wide variety of communication standards.

Hence, a bitrate adaptive CDR circuit able to operate in a wide range of bit rates from 312.5 Mb/s up to 2.5 Gb/s is proposed in this paper.

Circuit Description

In general, a CDR circuit contains a frequency-locked loop (FLL), a phase-locked loop (PLL) and a voltage-controlled oscillator (VCO). The FLL starts by comparing the frequency of the data stream with that of the VCO in order to drive their frequencies as close as possible. Next, the PLL performs a similar process to align their phases [2]-[3].

Fig. 2 shows the block diagram of the proposed multi-rate CDR circuit, where the FLL is formed by a digital coarse frequency detector (CFD) and a lock detector; while the phase-locked loop contains a linear PD and a charge pump. Two *LC*-VCO [4] both with a coarse control of 2^5 digital levels are multiplexed and fed into a digitally-controlled divider. This combination of VCO and divider allows to achieve a wide range of frequencies.

The frequency detector operates by counting the number of edges (both rising and falling) of the data stream over an entire clk period. As illustrated in the timing diagram of Fig. 3, if the frequency error, $\Delta f = (f_{clk} - f_{\mathrm{Din}})/f_{\mathrm{Din}}$, is big, then the number of data edges over a clk period will be high; as this difference decreases by making the clk period smaller for the same bit rate, the number of data edges counted in the clock period will decrease. This way, whenever a data edge occur within a clk period, the coarse frequency detector will send an UP signal to the VCO band selector, which will increase the frequency band by means of a 5-bit digital word.

The lock detector deactivates the VCO digital frequency band increment when a frequency error, Δf, reach a value small enough so the phase detector is able to properly operate. Then, the FLL is disabled and the PLL takes control to start the phase locking process.

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Results

The proposed adaptive bitrate CDR circuit has been designed in a standard 0.18-µm CMOS technology and is fed with a single supply voltage of 1.8 V; it covers data bit rates from 312.5 Mb/s to 2.5 Gb/s without dead-zones, with a maximum power consumption of 140 mW at 2.5 Gb/s.

The digital frequency locking of the CFD block for the minimum and maximum bit rates is shown in Fig. 4, where it can be seen that the final frequency error achieved, Δf, is below 7%. For the phase acquisition, this difference relaxes the design complexity of this block since most of the proposed architectures have a bigger pull-in range. Hence, the proposed CDR circuit employs a Hogge PD for the second loop [5]. Its its operation consists in sampling the input data stream by the two flanks of the clock through two D-type flip-flops to generate replicas of the data with certain delays; one of these delays is determined by the phase difference between the data and the clock, whereas the other one is fixed at one half of the clock period; this clk-based delay gives the Hogge PD a phase capture range from $-\pi$ to π.

Finally, Fig. 5 shows the complete transient response for both the frequency and phase at the minimum and maximum bit rates. (312.5 Mb/s and 2.5 Gb/s, respectively). As can be seen, the total locking time is below 13µs.

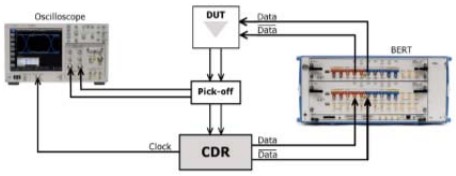

Fig. 1. Clock and Data Recovery (CDR) circuit in communication signal analyzers.

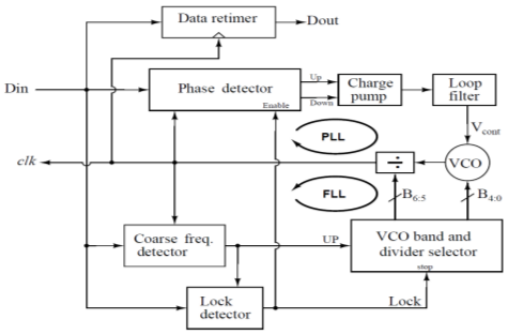

Fig. 2. Block diagram of the proposed adaptive CDR circuit.

Conclusions

An adaptive bitrate clock and data recovery circuit is presented in this paper. The circuit has been simulated in a standard CMOS technology, where is shown that is able to work from 312.5 Mb/s to 2.5 Gb/s without any external tuning. The described methodology is valid for wider ranges with the limit set by the speed of the VCO.

References

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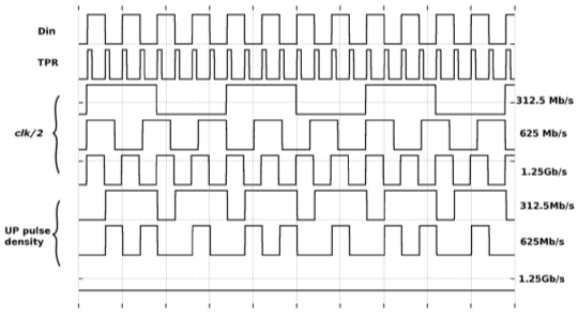

Fig. 3. Timing diagram of the coarse frequency detector for an 1.25 Gb/s NRZ and clock frequencies from312.5 MHz to 1.25 GHz.

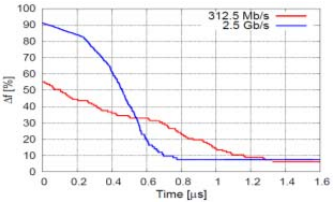

Fig.4 Digital frequency locking for minimum (312.5 Mb/s) and maximum (2.5 Gb/s) bit rates.

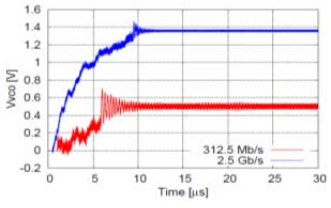

Fig.5 Frequency and phase locking for minimum (312.5 Mb/s) and maximum (2.5 Gb/s) bit rates.